

MODEL NAME : FAF00

PCB NO : LA-6961P ( DA\*\*\*\*\* )

BOM P/N : TBD

# Dell/Compal Confidential

## Schematic Document

Phantom (Huron River)

Sandy Bridge (BGA1023) + Cougar Point (SFF)

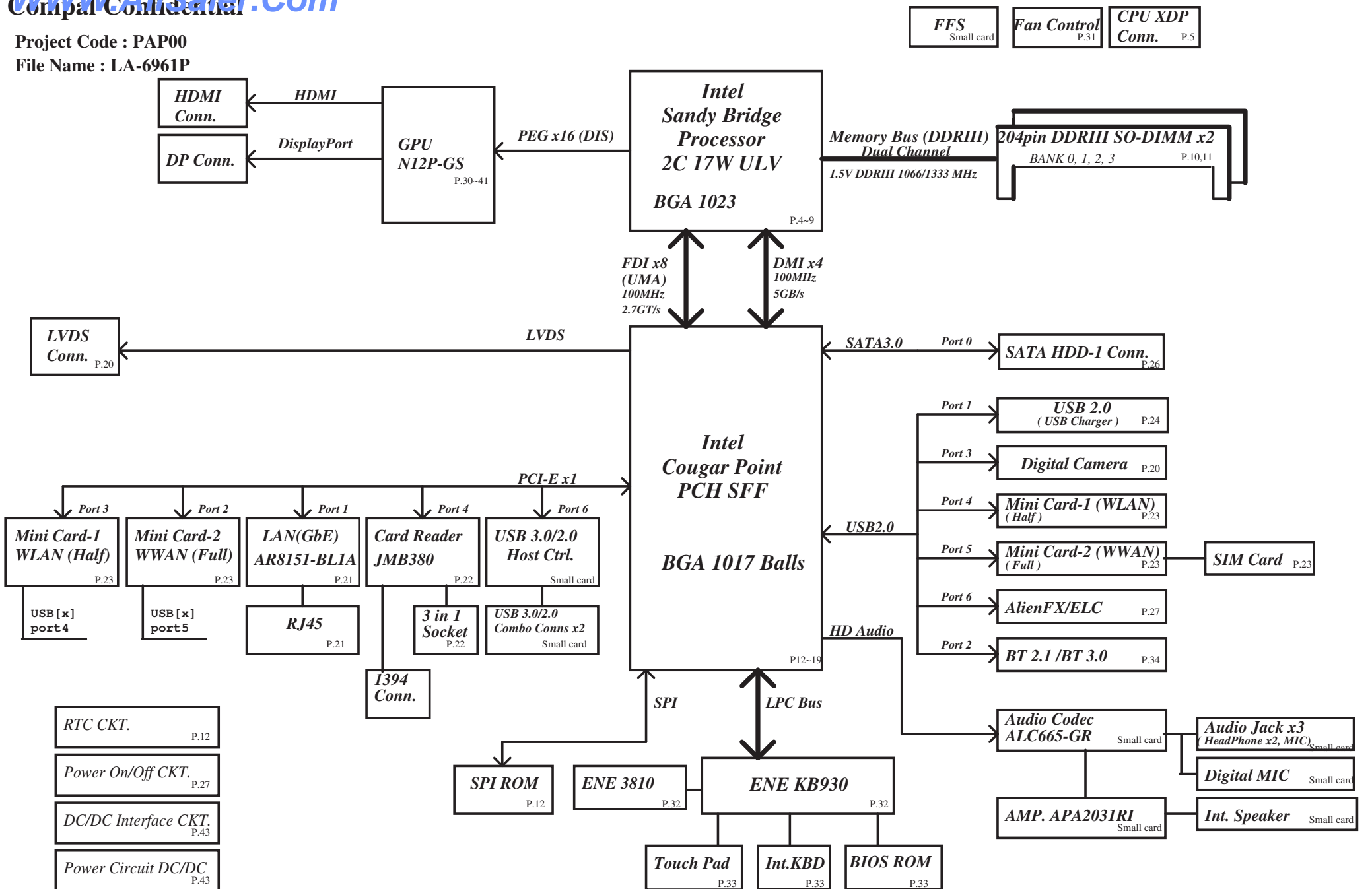
DISCRETE VGA N12P-GS (optimus)

2010-11-29

Rev: 0.4

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Project Code : PAP00  
File Name : LA-6961P



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Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	FFS	VGA Thermal Sensor	SMSC
EC_SMB_CK1 EC_SMB_DA1	KB930			V					
EC_SMB_CK2 EC_SMB_DA2	KB930								
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH	V	V			V		V	V
MEM_SMBCLK MEM_SMBDATA	PCH				V		V		

Link

PCH



USB PORT#	DESTINATION
0	None
1	JUSB1 (Ext Left Side)
2	Bluetooth
3	CAMERA
4	JMINI1 (WLAN)
5	JMINI2 (WWAN)
6	ELC
7	None
8	None
9	None
10	None
11	None
12	None
13	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	None
PCI4	None

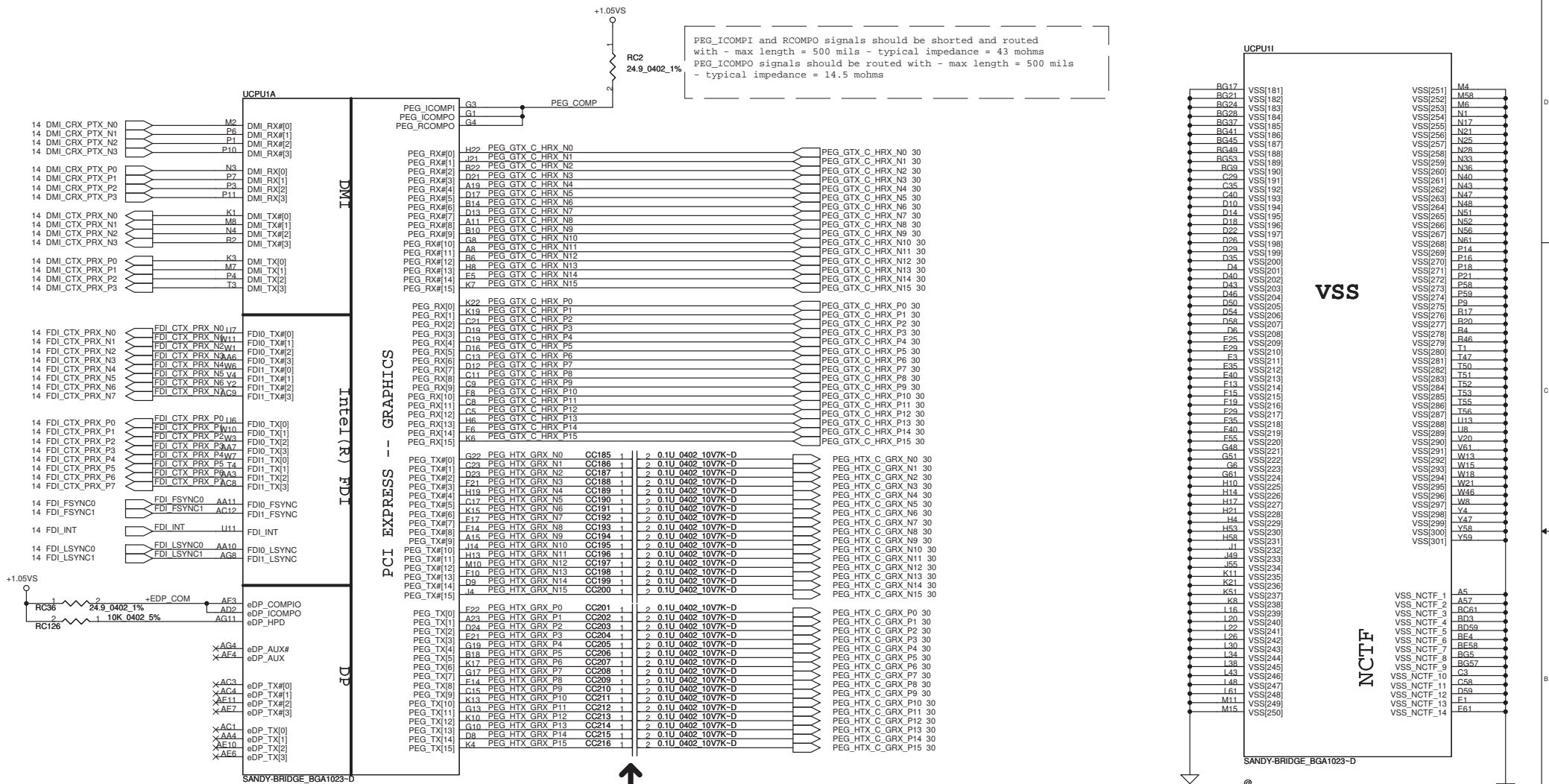
SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	None
SATA3	None
SATA4	None
SATA5	None

Symbol Note :

 : means Digital Ground  
 : means Analog Ground

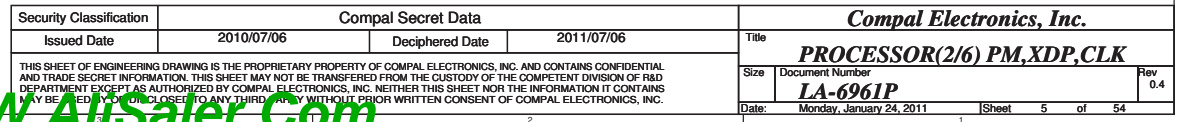
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER and 1394
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

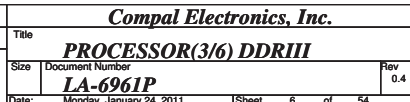
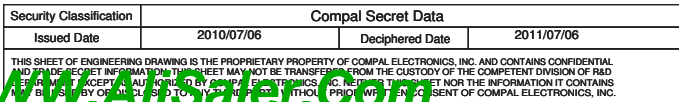
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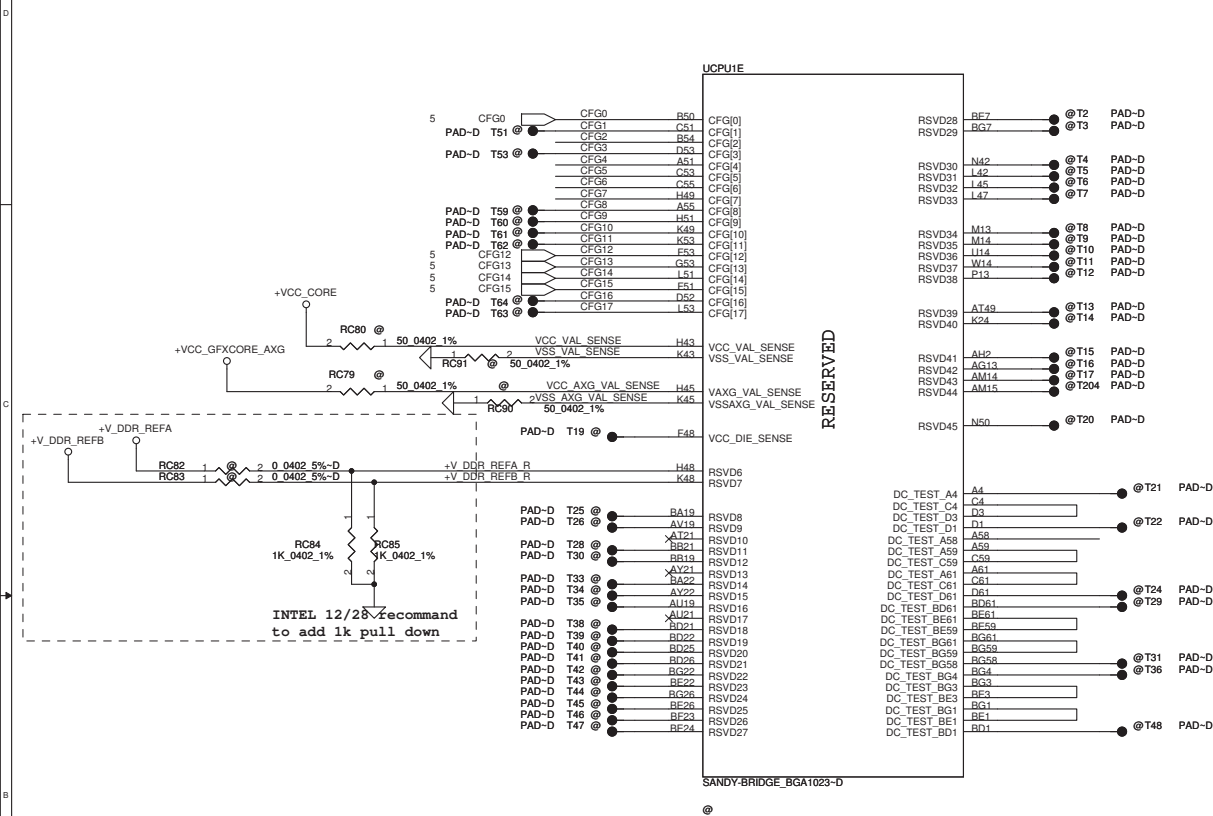


Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

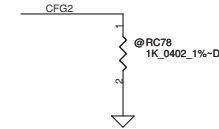
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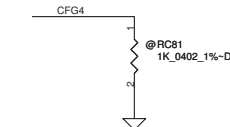




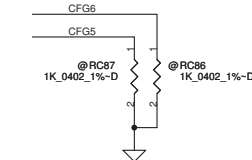
## CFG Straps for Processor



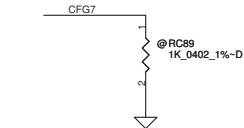
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	*1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

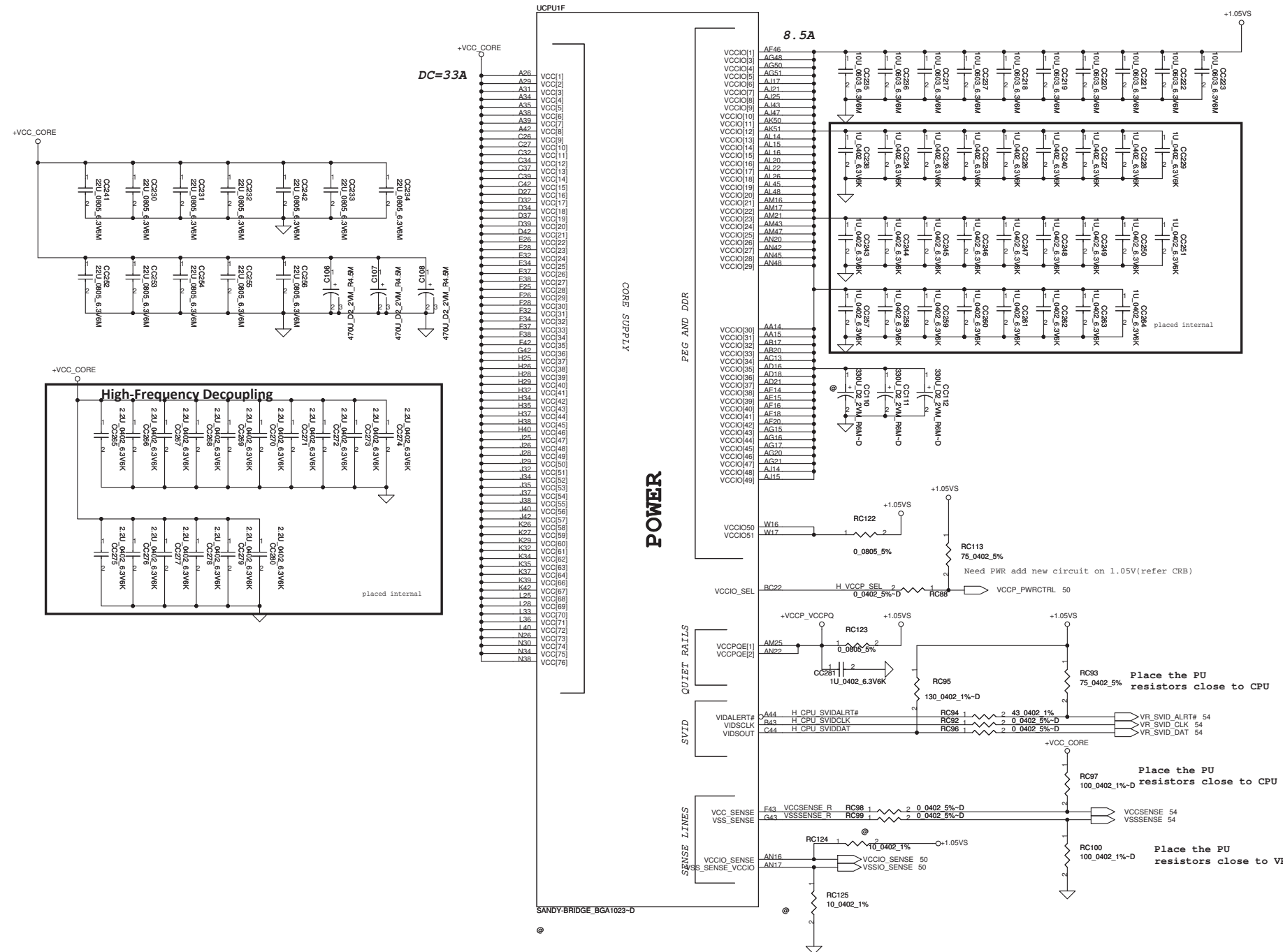


PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



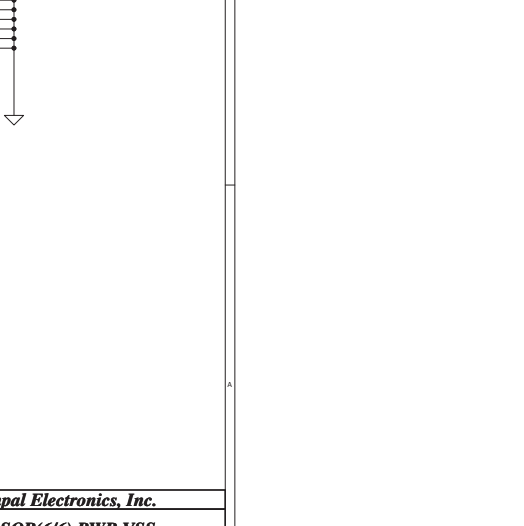
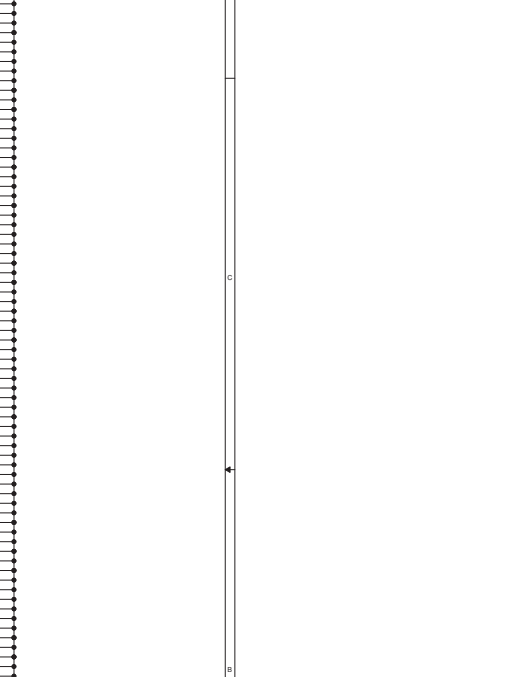
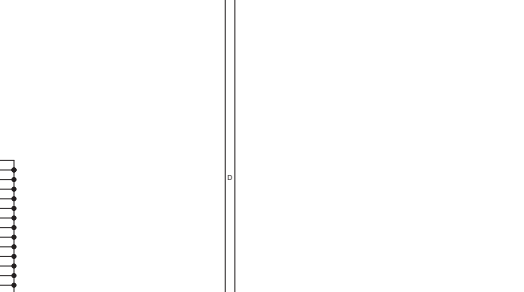
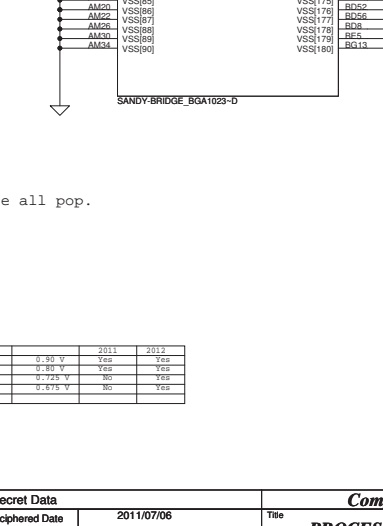
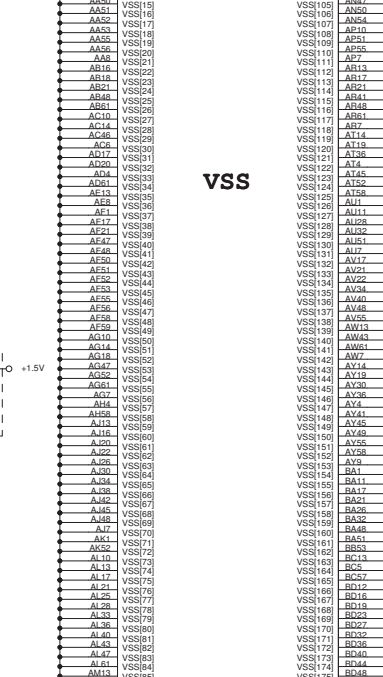
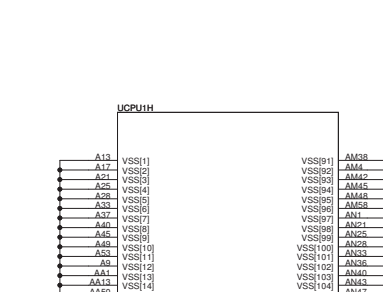
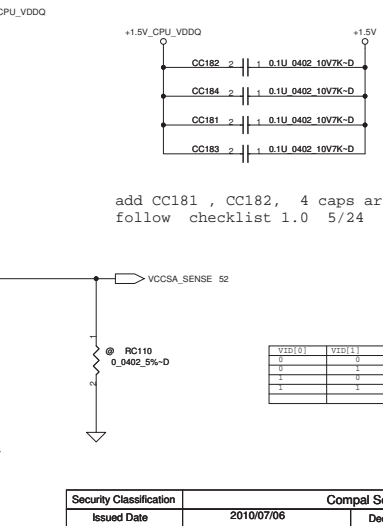
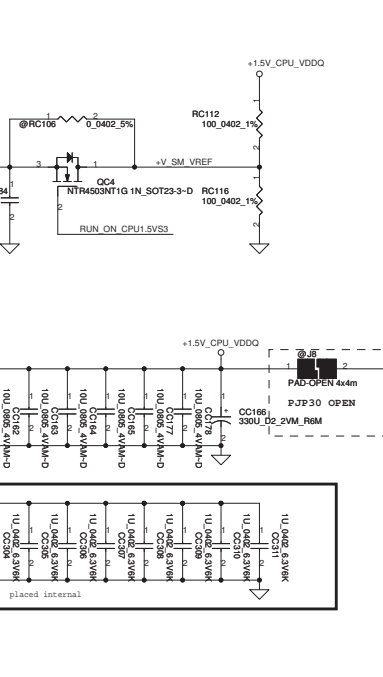
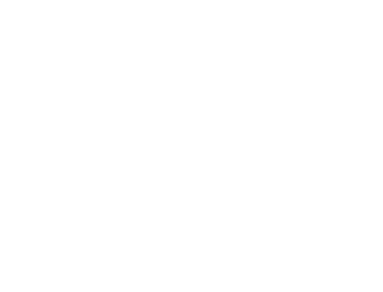
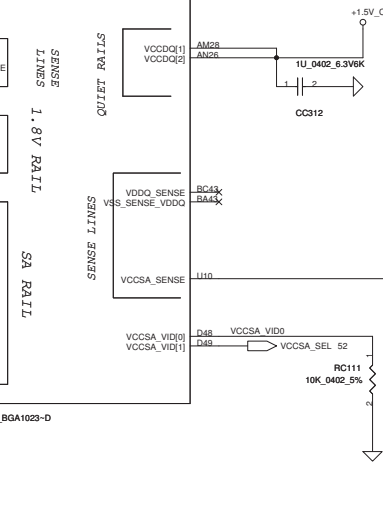
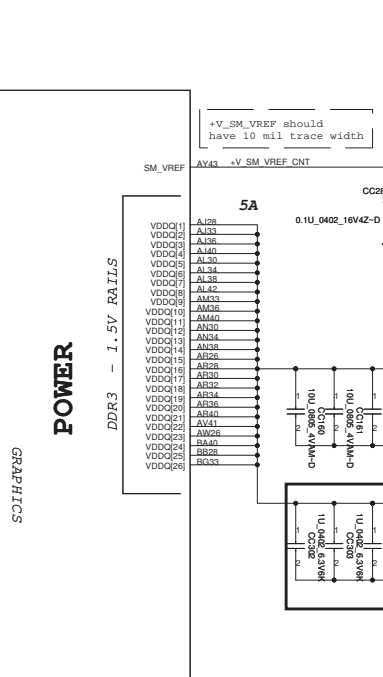
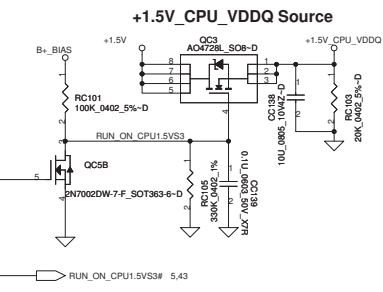
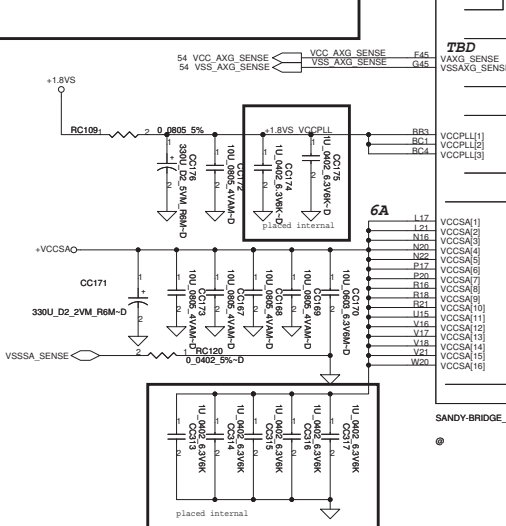
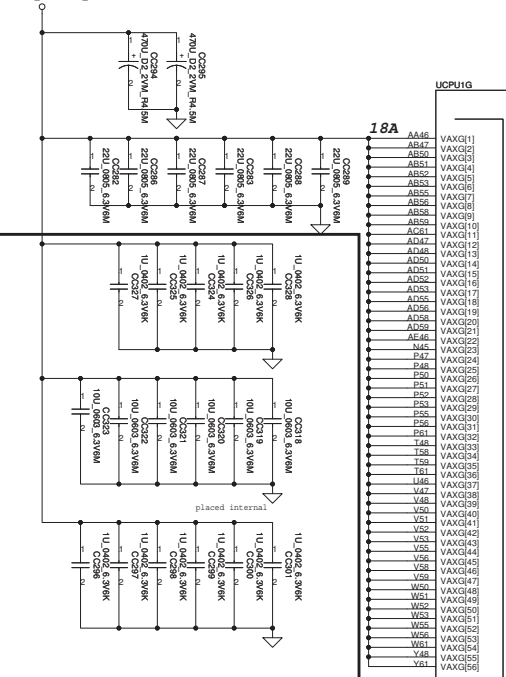
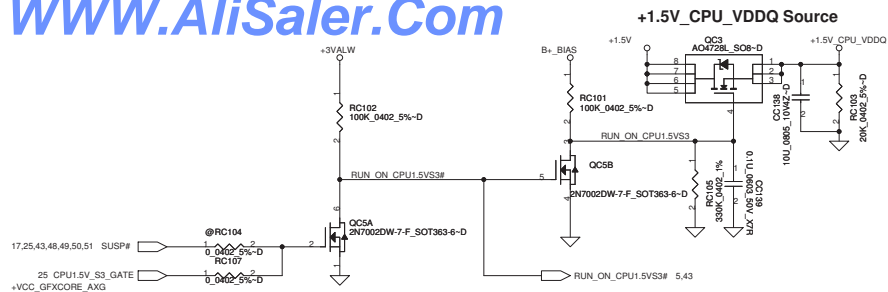
PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





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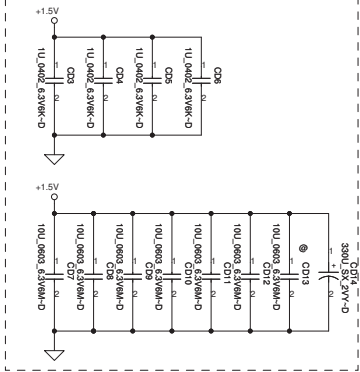
add CC181 , CC182 , 4 caps are all pop.  
follow checklist 1.0 5/24

VDDQ(0)	VDDQ(1)	2011	2012
0	0	0.30 V	Yes
1	1	0.30 V	Yes
2	2	0.30 V	Yes
3	3	0.30 V	Yes

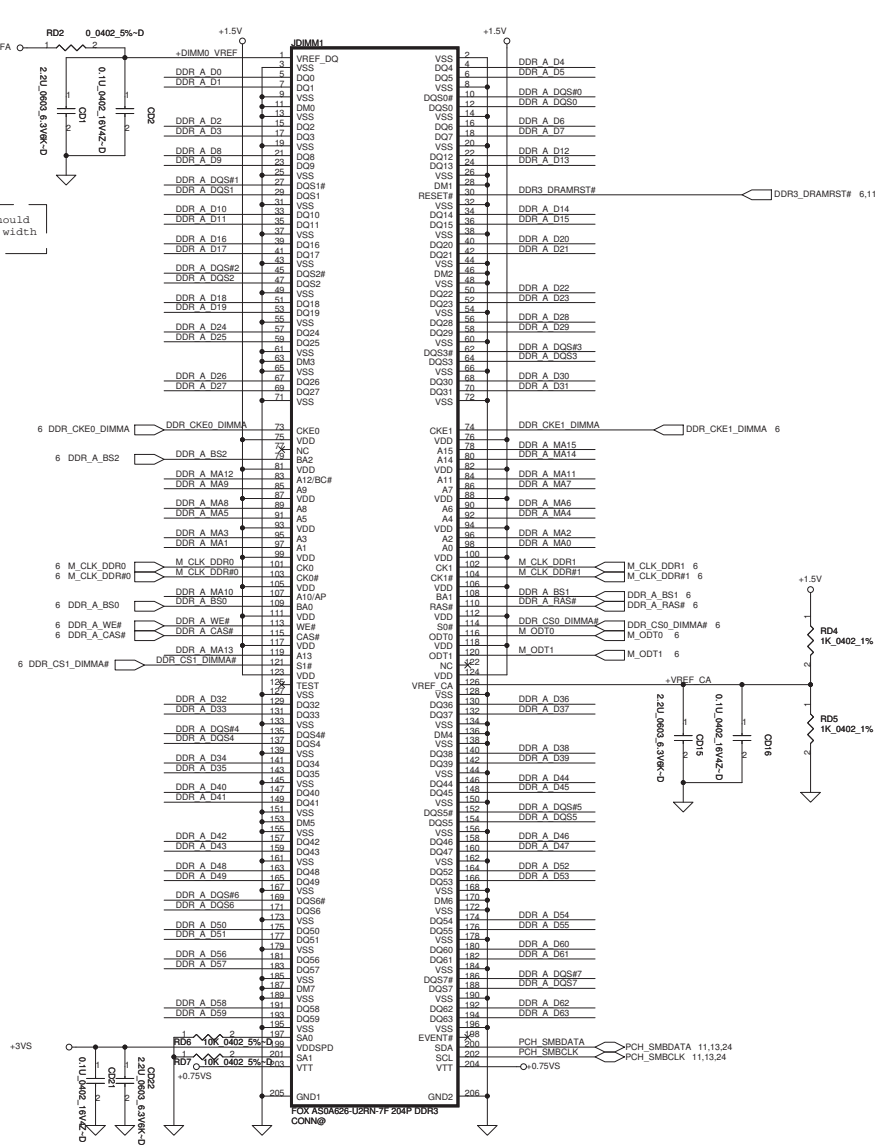
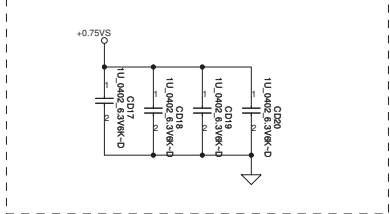
DDR\_A\_CS#(0..7)  
DDR\_A\_DQ[0..63]  
DDR\_A\_MA[0..15]

Layout Note:  
Place near JDIMM1

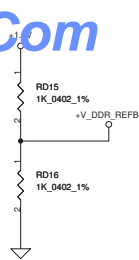
All VREF traces should  
have 10 mil trace width



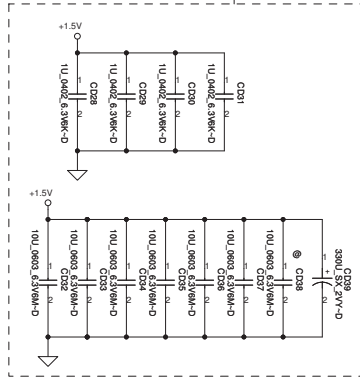
Layout Note:  
Place near JDIMM1.203,204



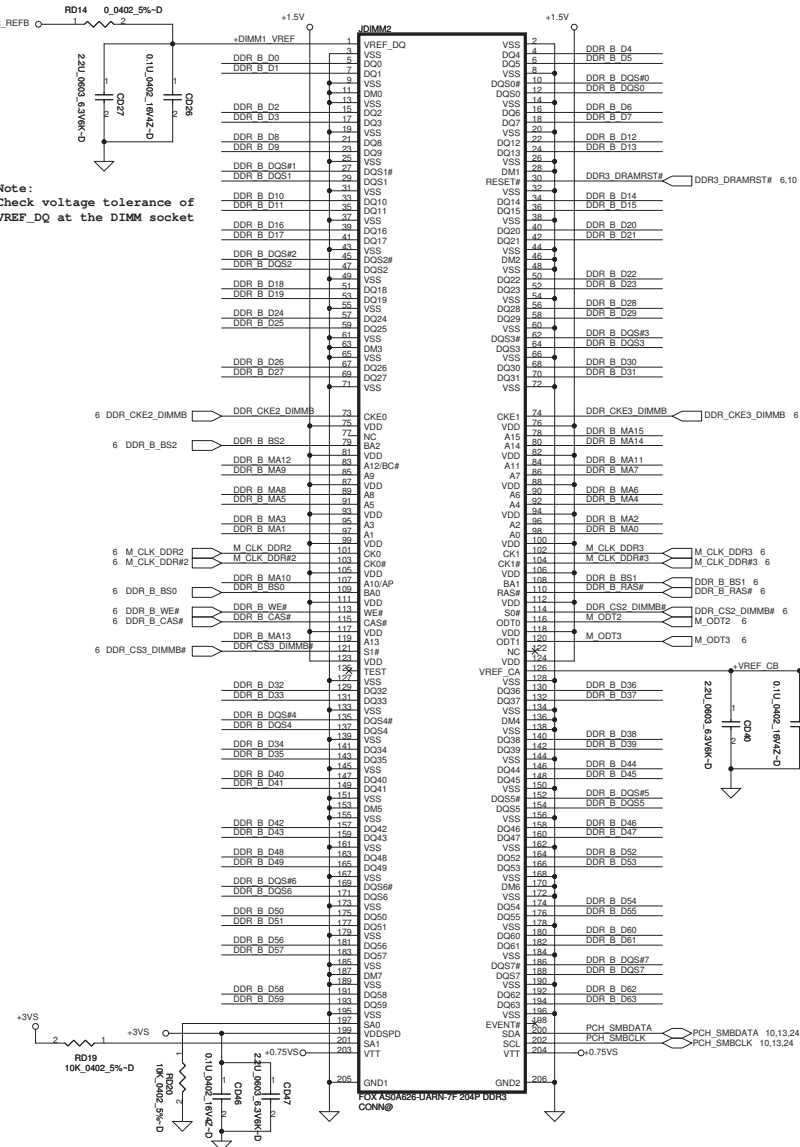
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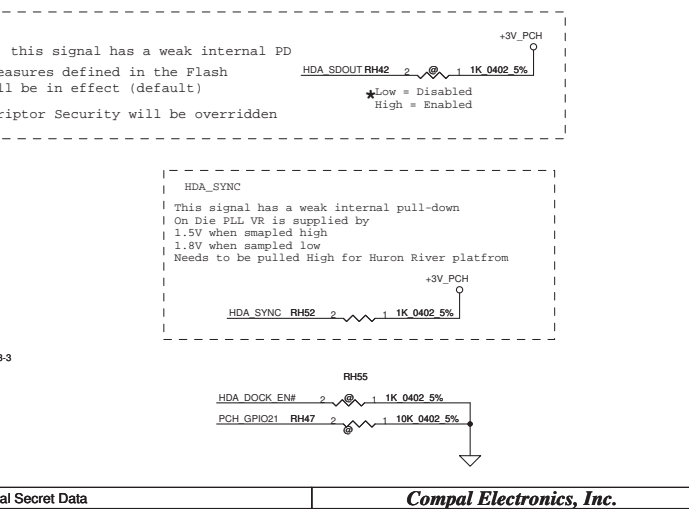
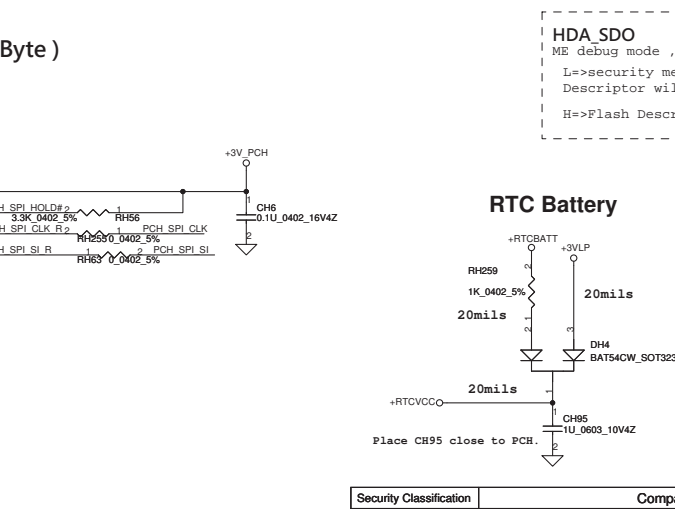
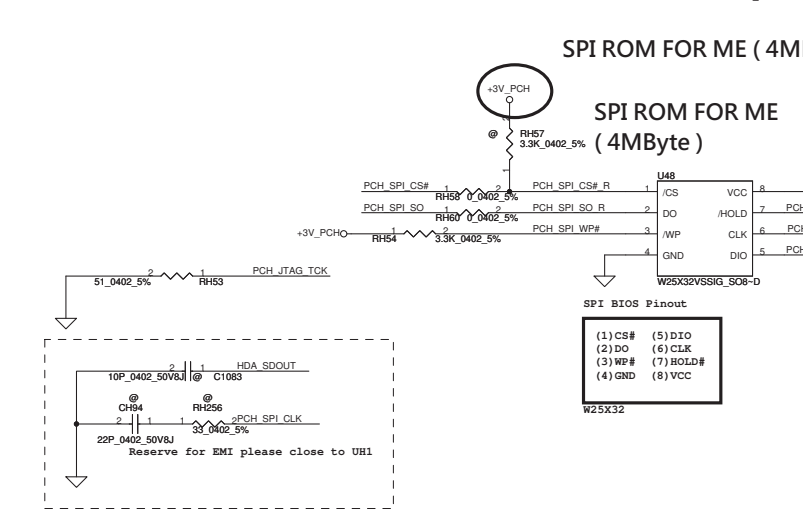
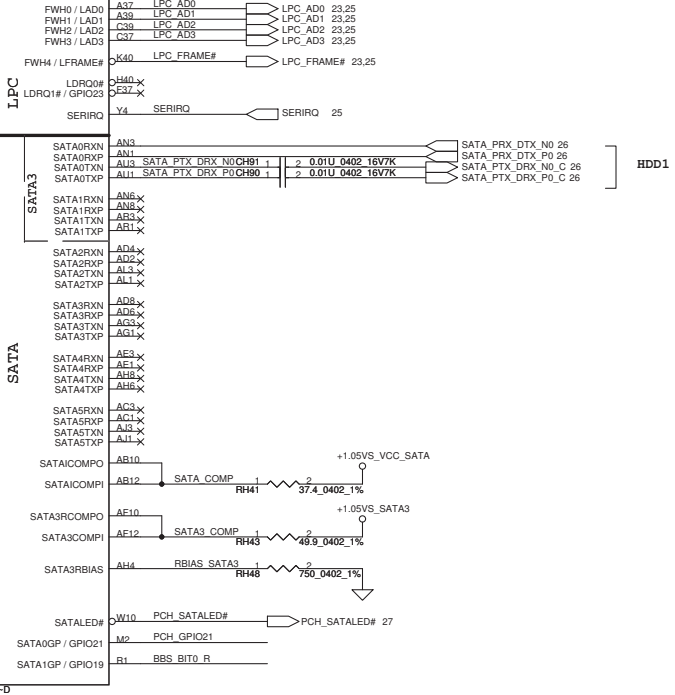
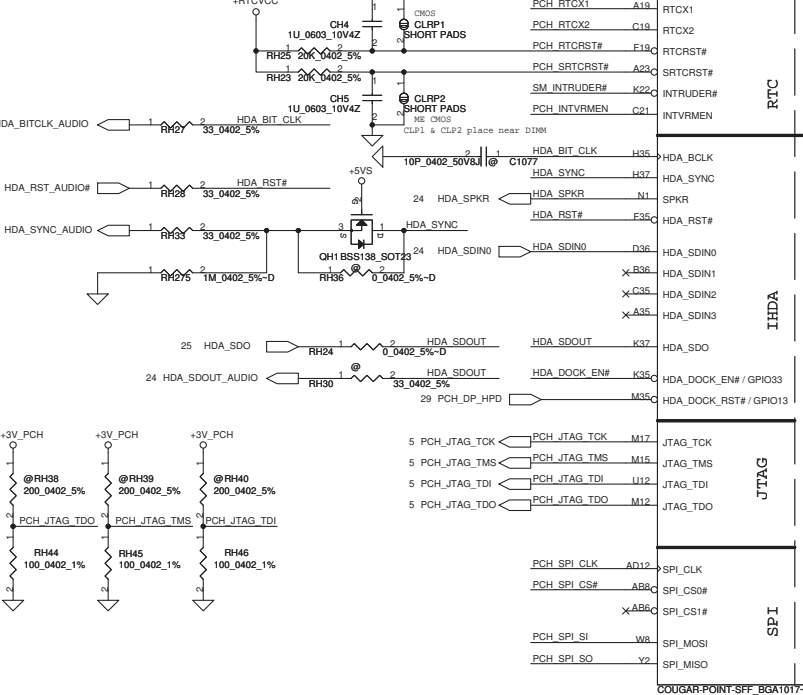
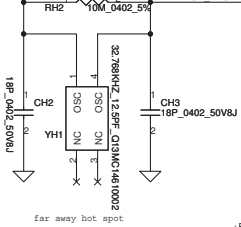
All VREF traces should have 10 mil trace width



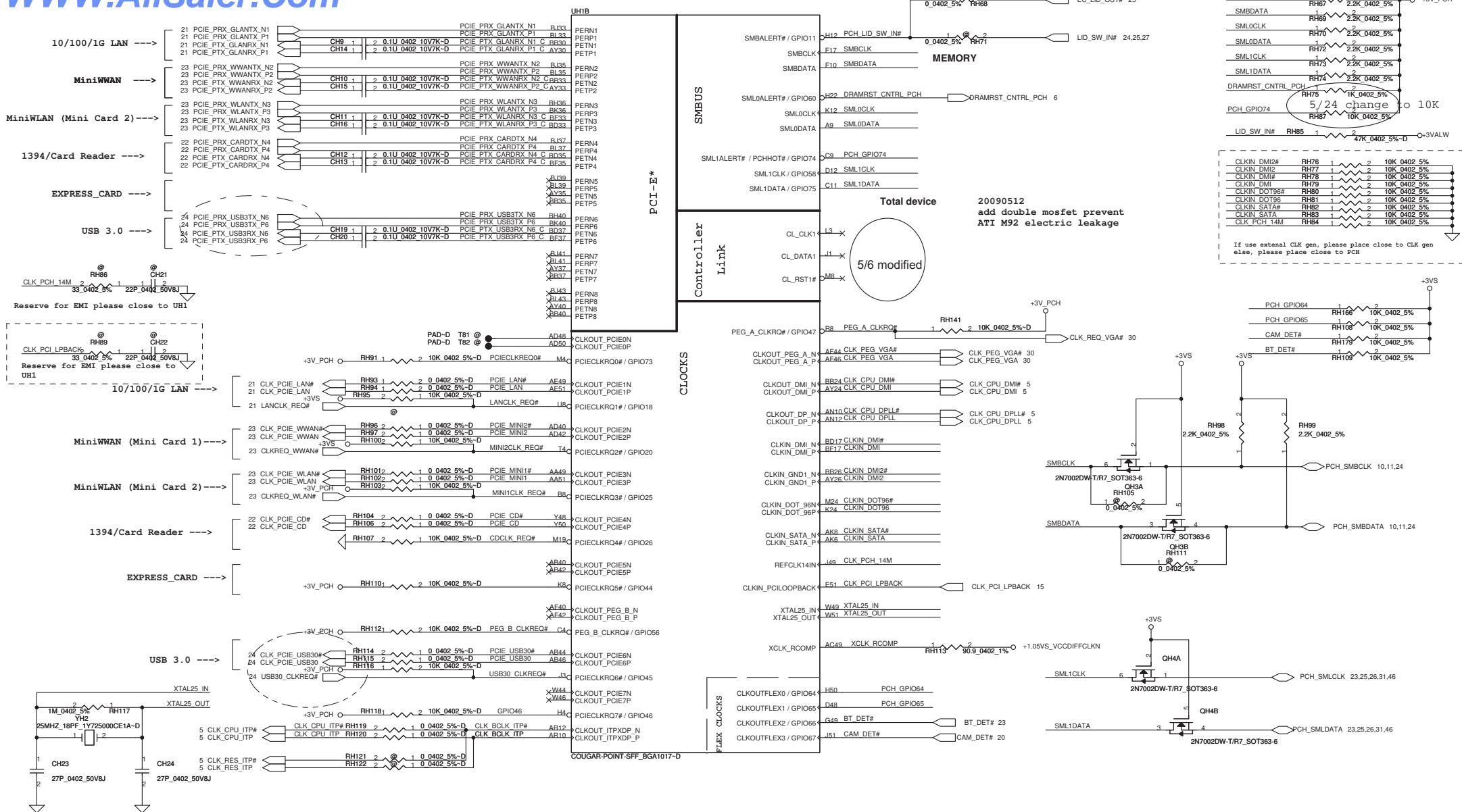
The circuit diagram shows a +0.75V source connected to a series combination of capacitors CD42 and CD45. This is followed by a parallel network of capacitors CD43 and CD44, and finally a parallel network of capacitors CD41 and CD46, all connected to ground.



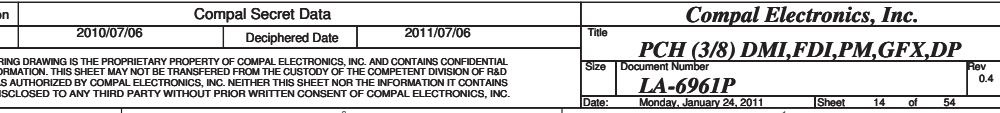
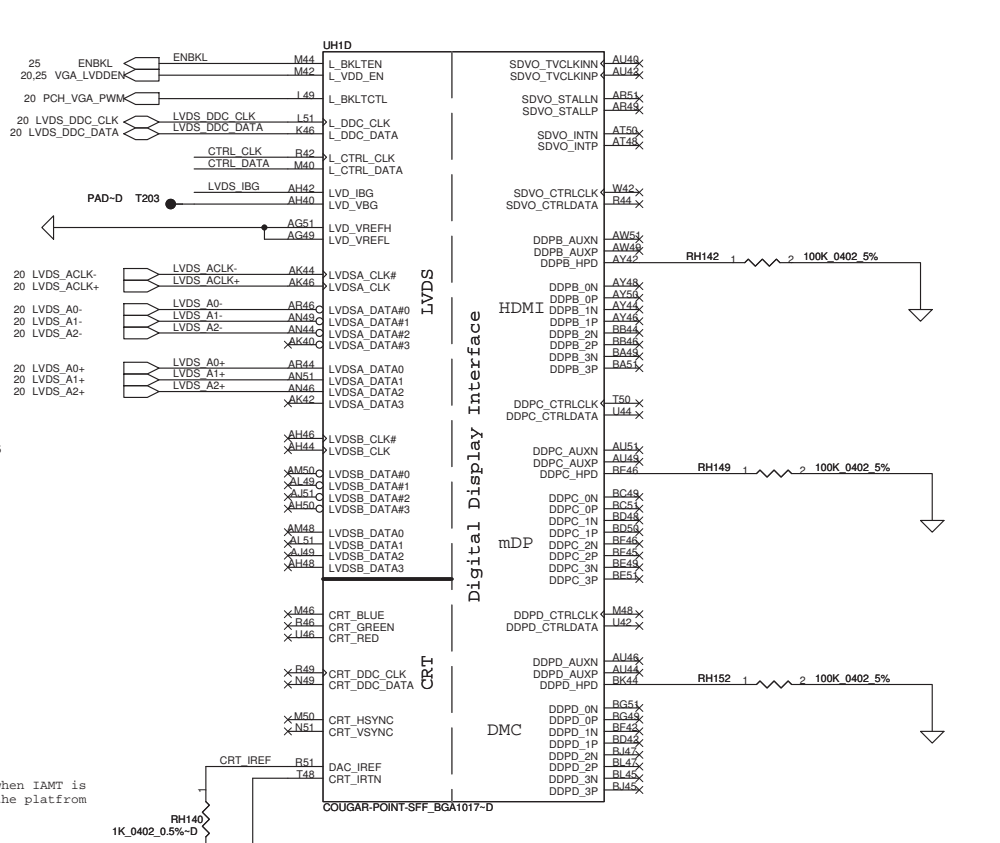
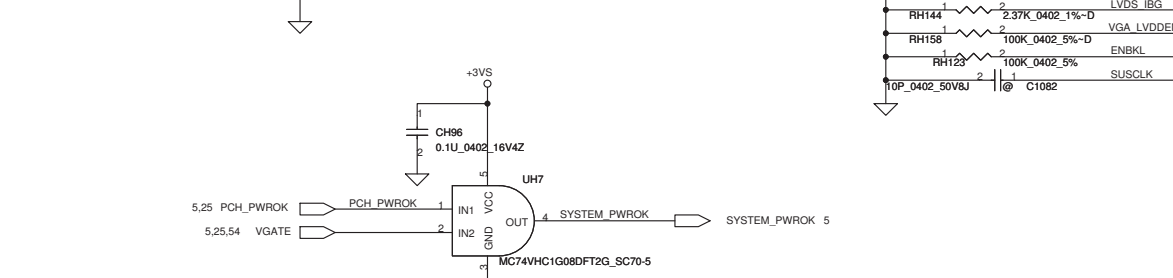
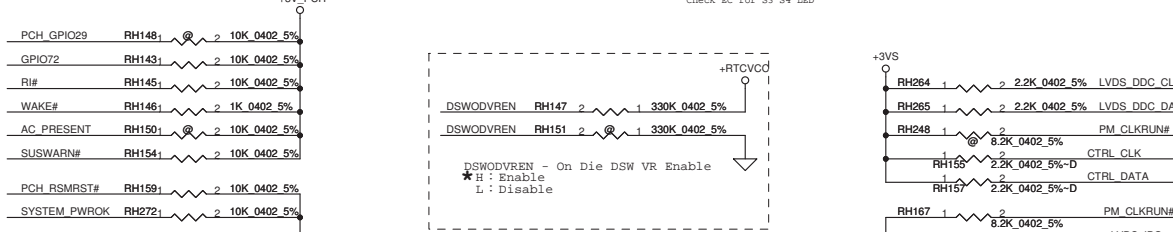
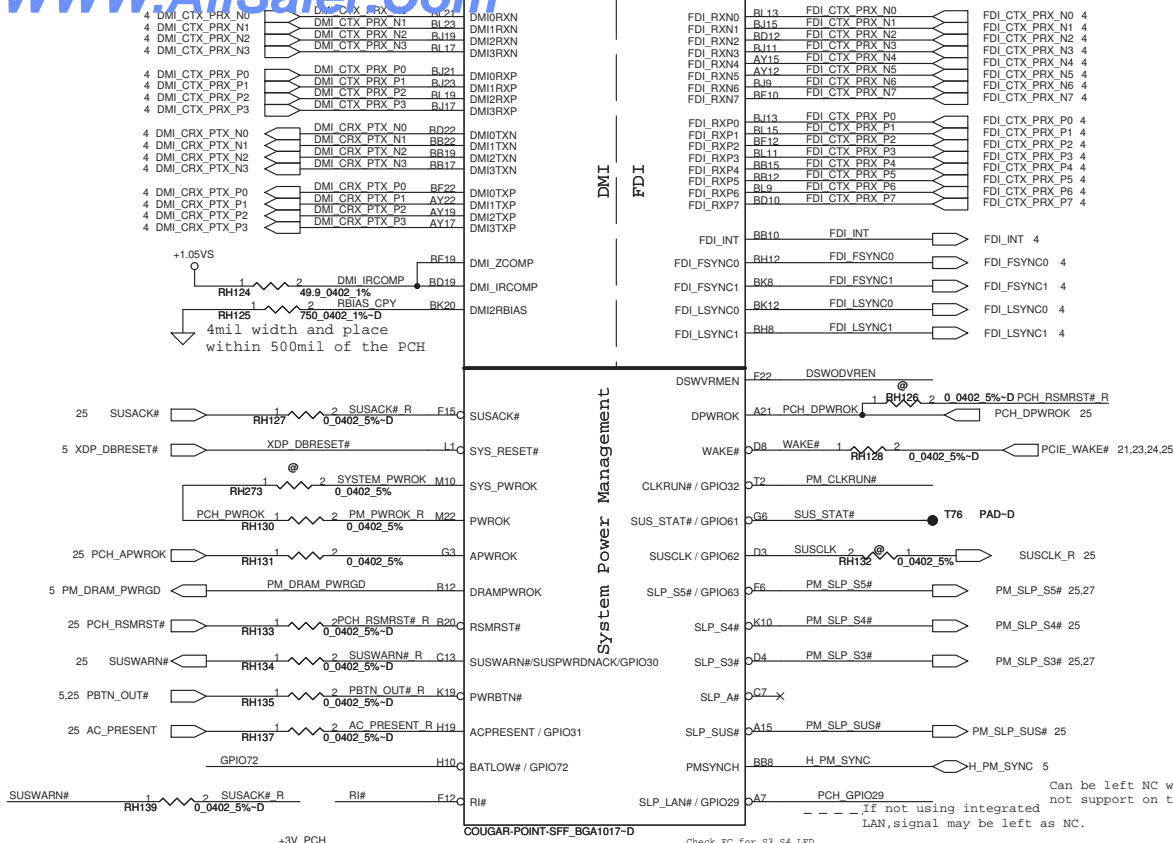
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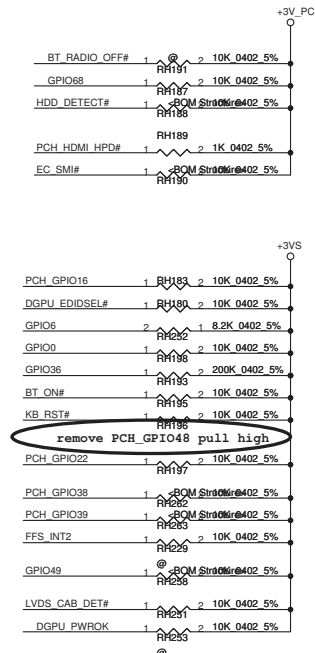


U1028  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up  
★ H: On-Die voltage regulator enable  
L: On-Die PLL Voltage Regulator disable

PCH\_GPIO37  
FDI TERMINATION VOLTAGE OVERRIDE  
★ LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)

PCH\_GPIO27 (Have internal Pull-High)  
★ High: VCCVRM VR Enable  
Low: VCCVRM VR Disable

PCH\_GPIO28 needs to be connected to XDP\_FN8  
PCH\_GPIO35 needs to be connected to XDP\_FN9  
PCH\_GPIO15 needs to be connected to XDP\_FN16  
  
Please refer to Huron River Debug Board DG 0.5

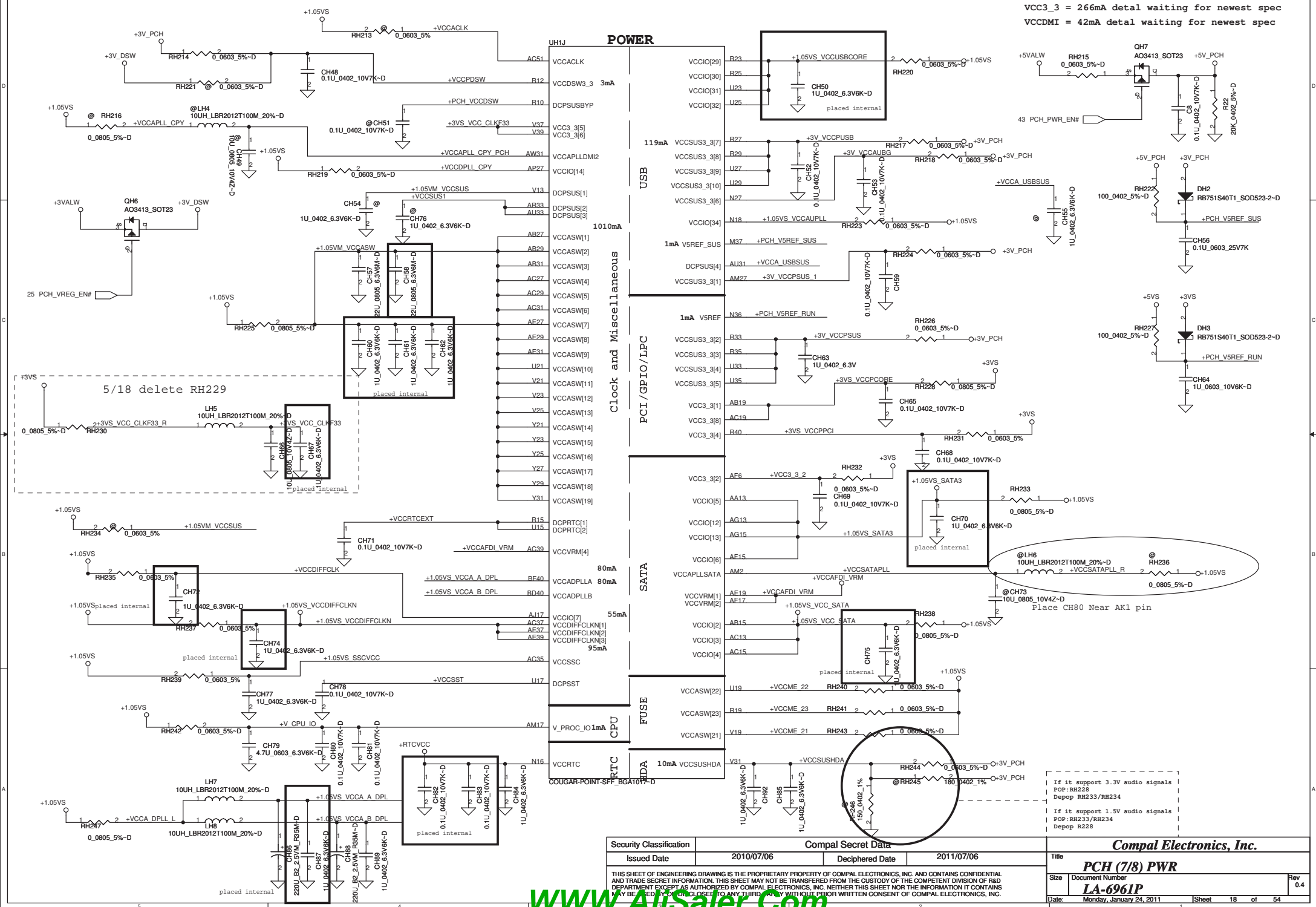


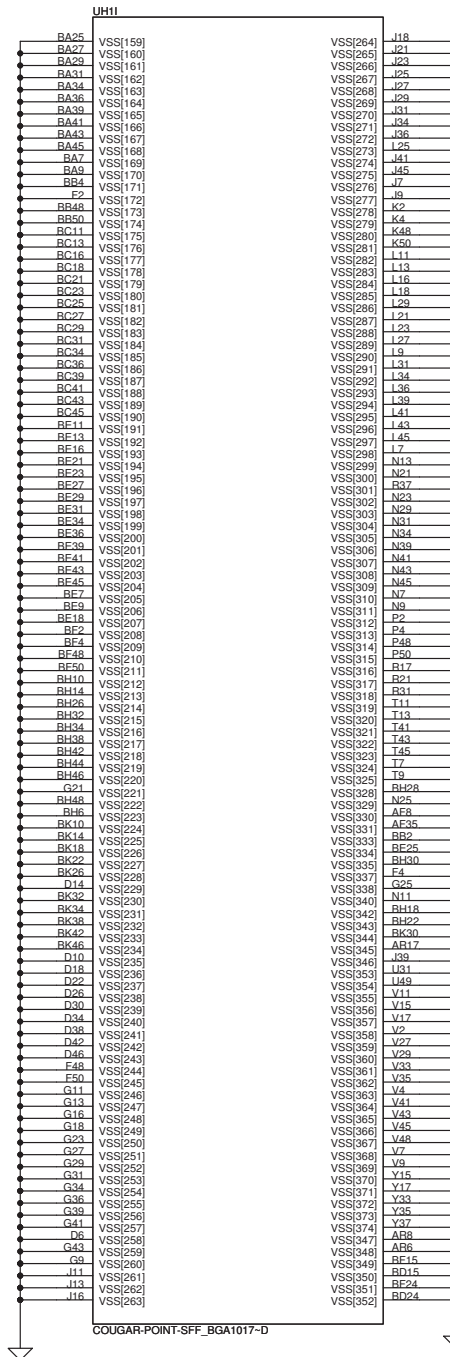
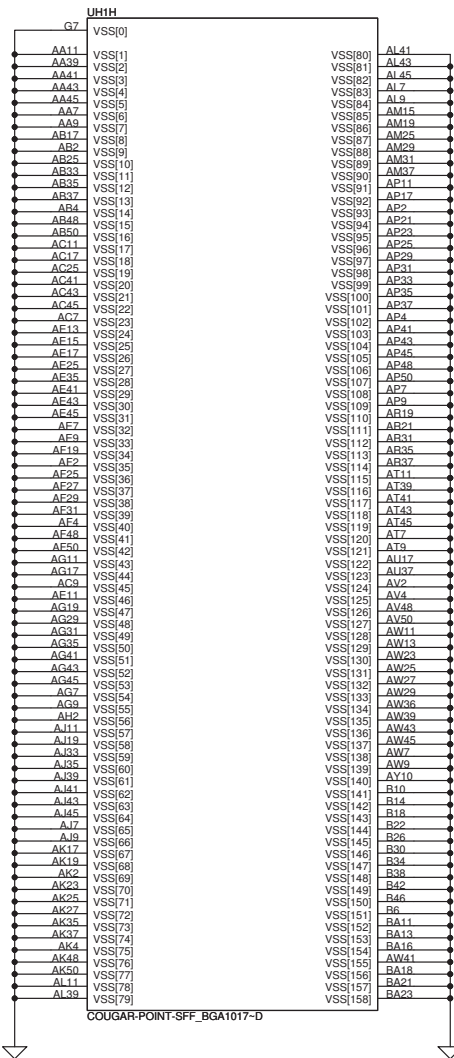
add RH185, RH229, RH251  
5/25

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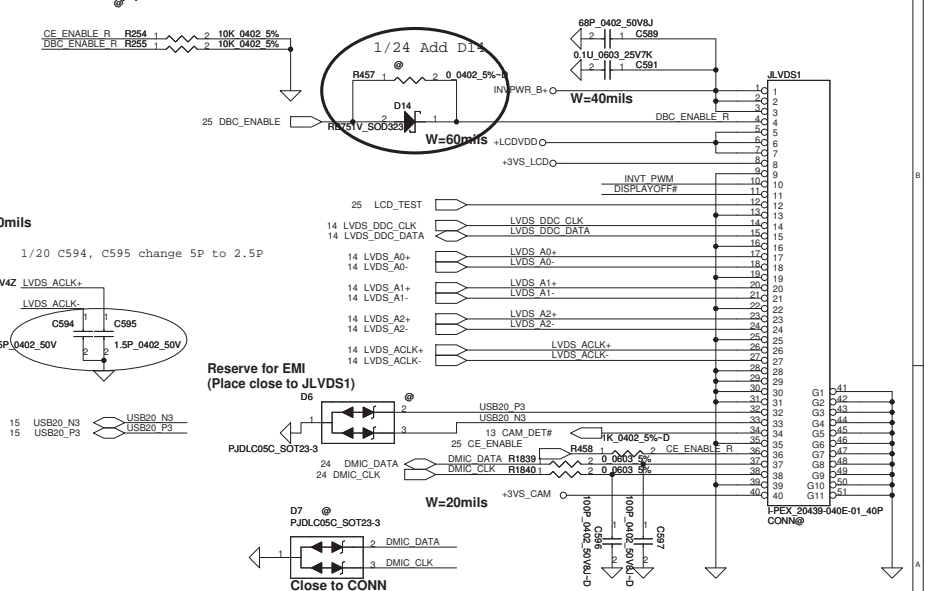
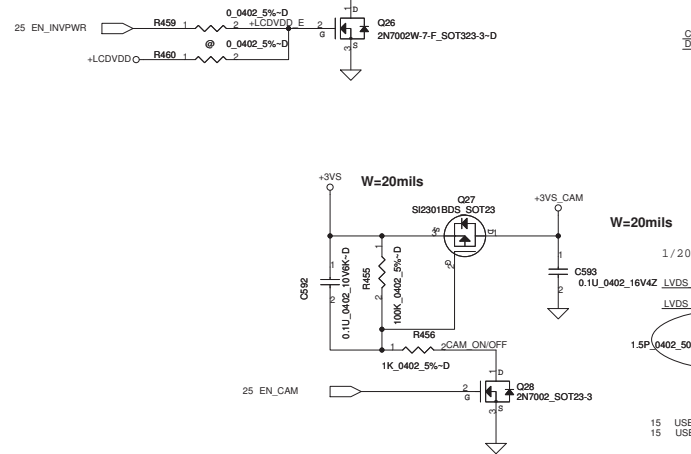
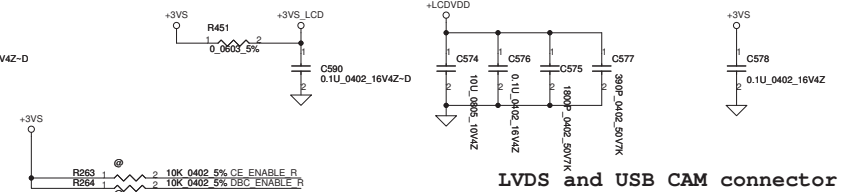
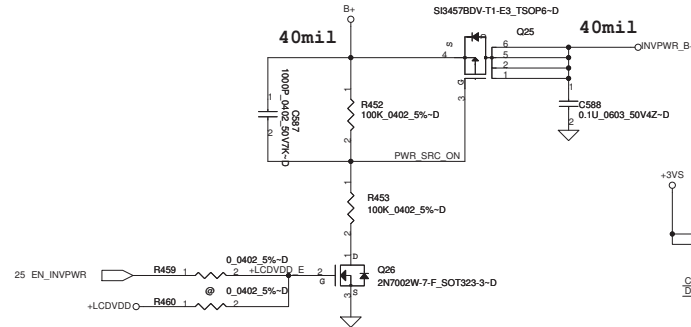
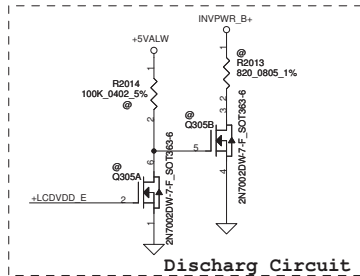
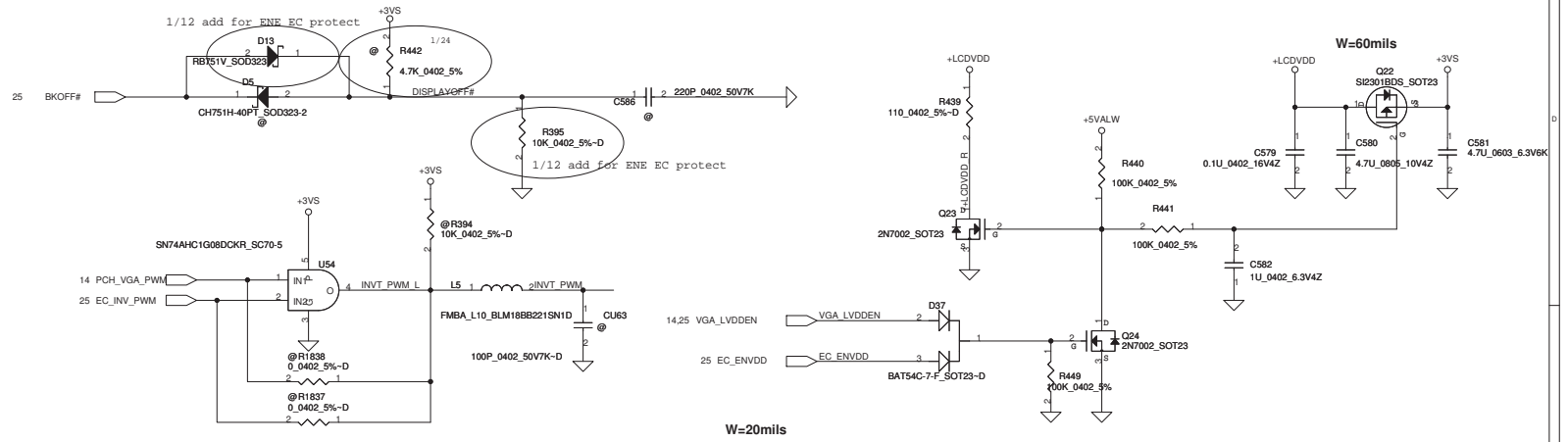


<b>Compal Electronics, Inc.</b>			
Title			
<b>PCH (6/8) PWR</b>			
Size	Document Number		Rev
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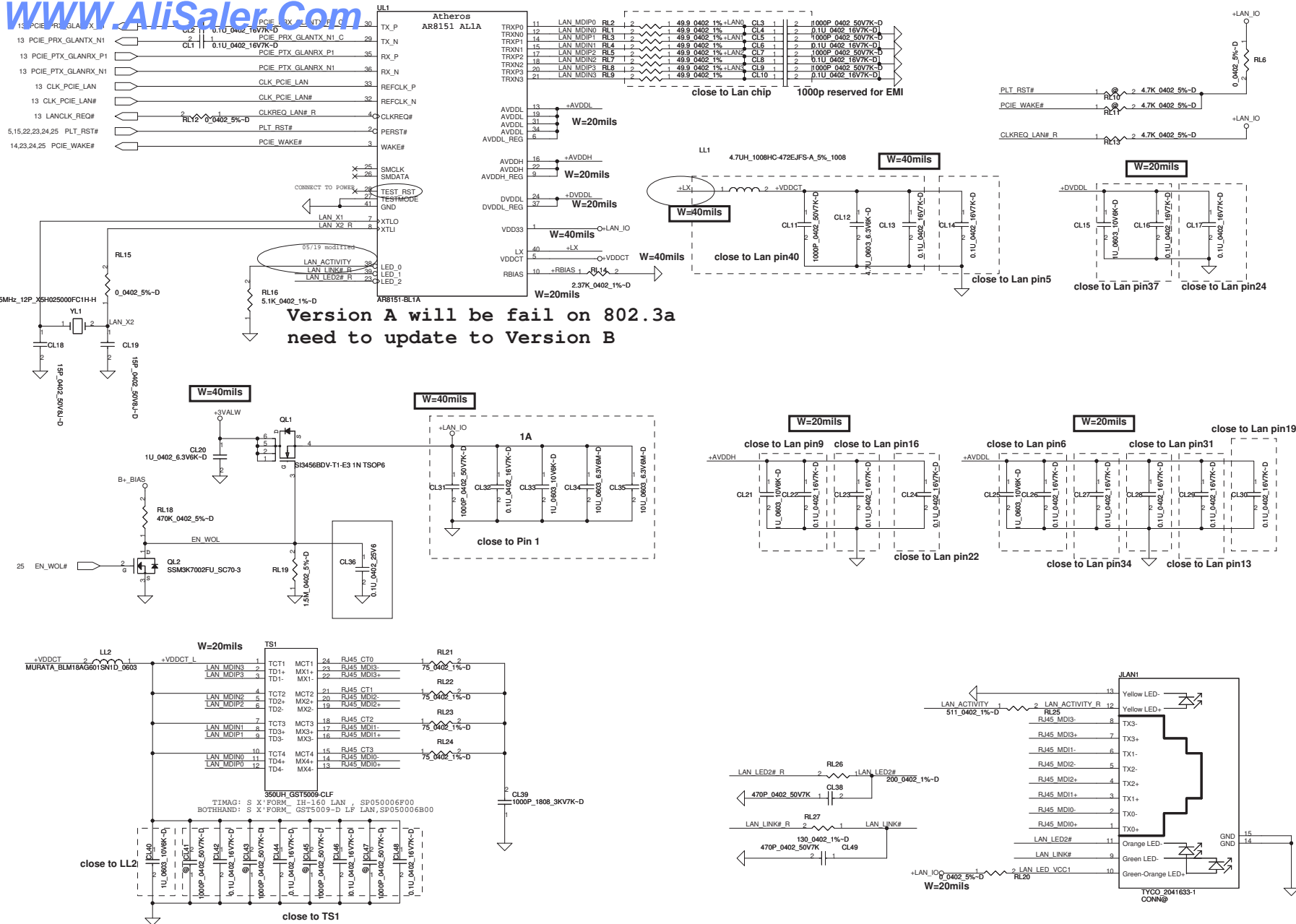




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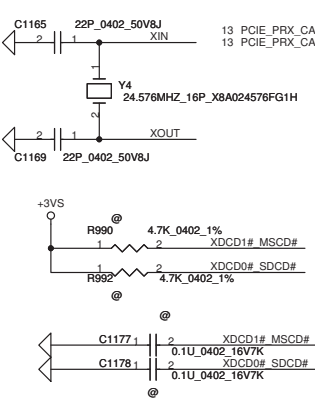
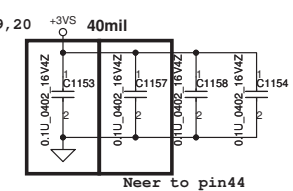
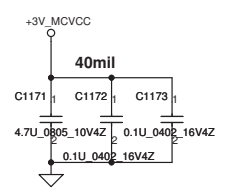
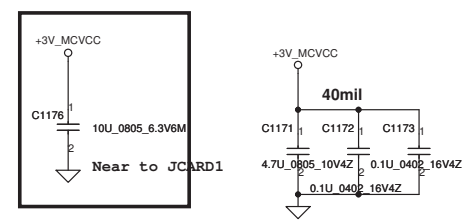
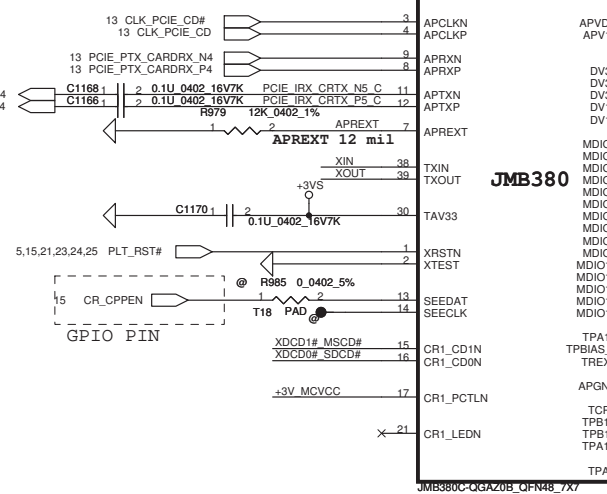
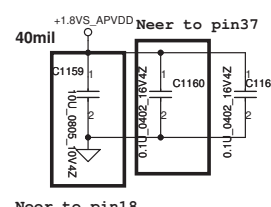
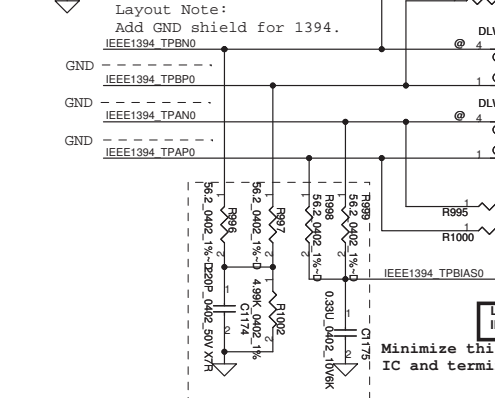
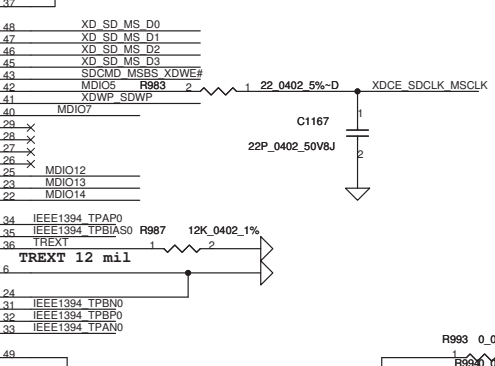
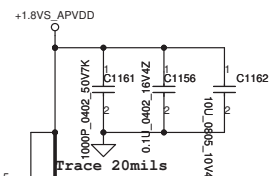
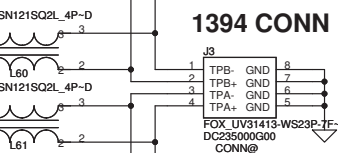
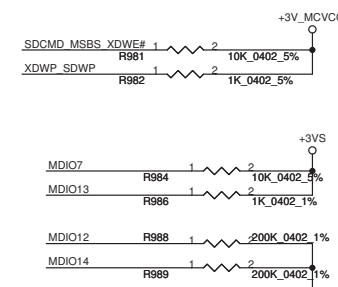
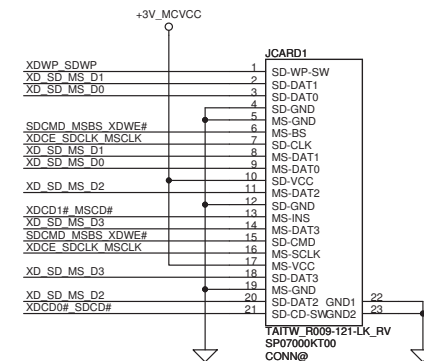


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### 3 in 1 Card Reader CONN

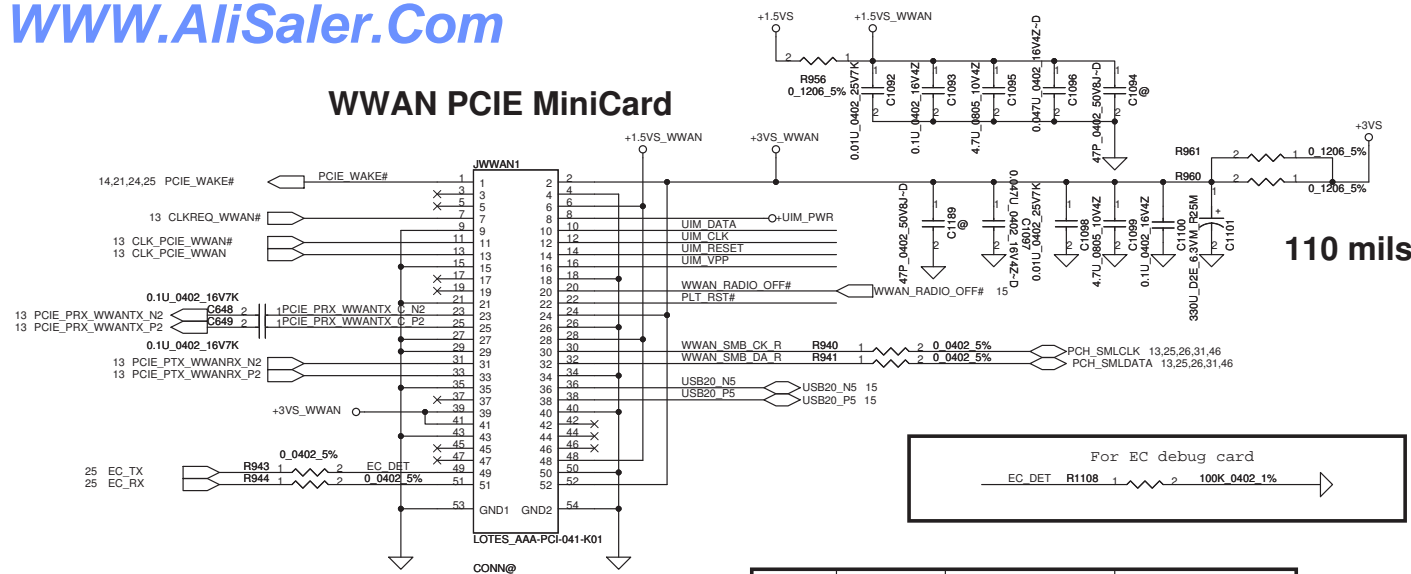


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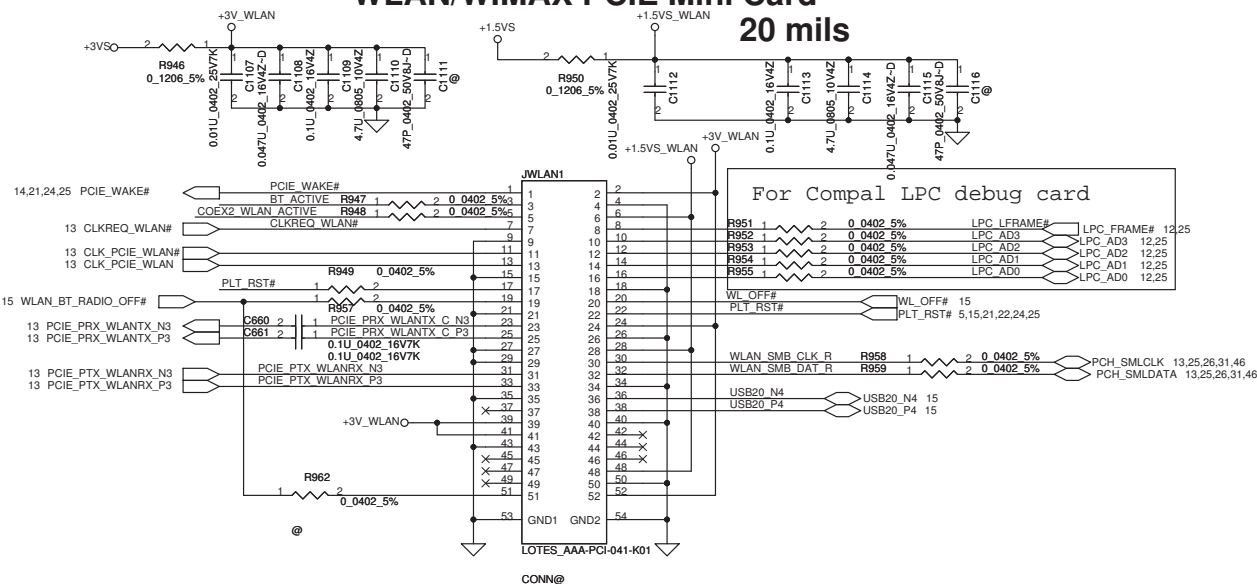


## WWAN PCIE MiniCard

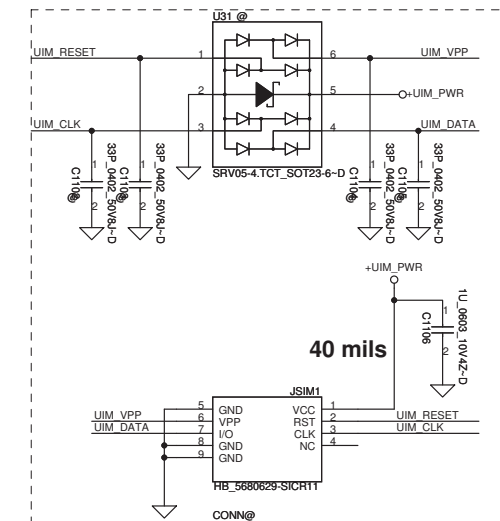


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+~9%	1000	750	
+3.3Vaux	+~9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+~5%	500	375	NA

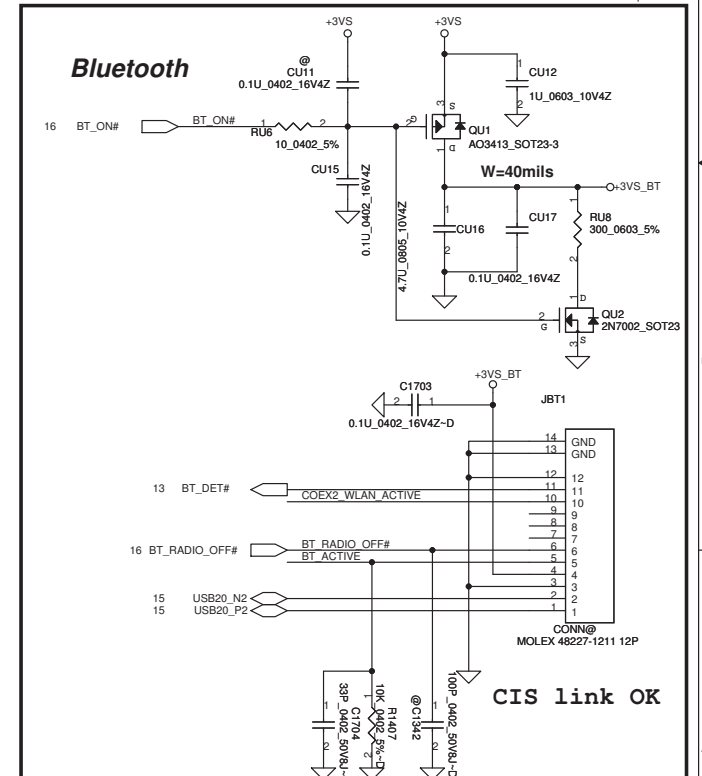
## WLAN/WIMAX PCIE Mini Card



## SIM Card



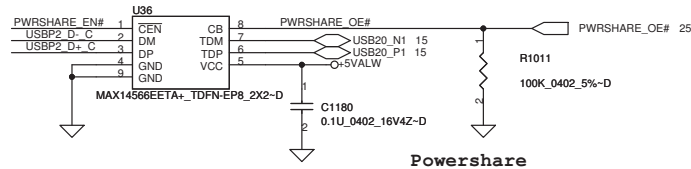
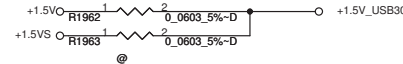
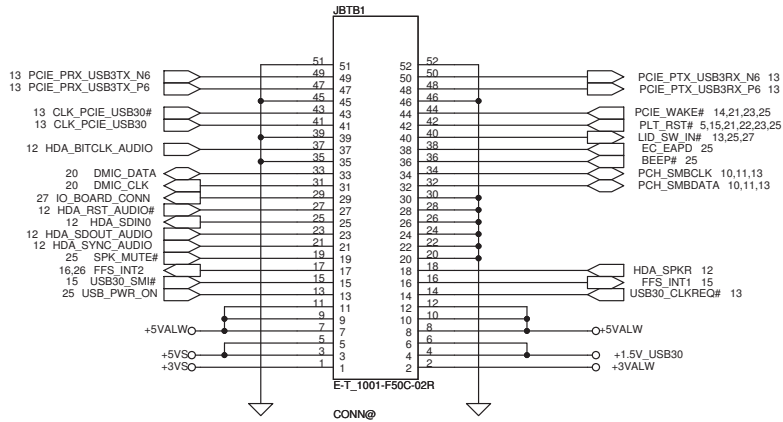
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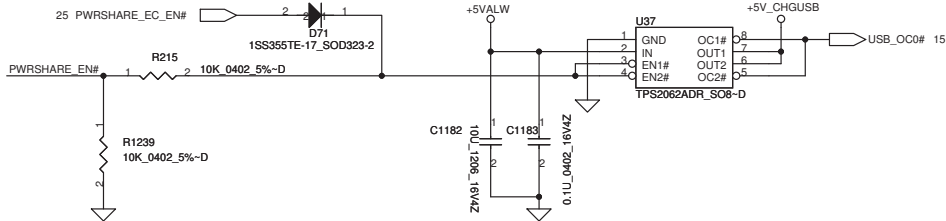
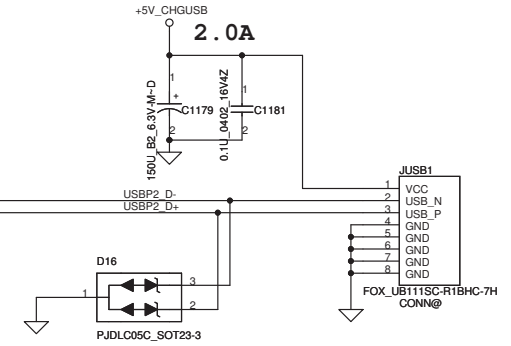
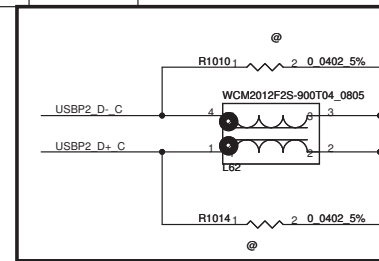
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Size	Document Number	Date		Sheet	Rev
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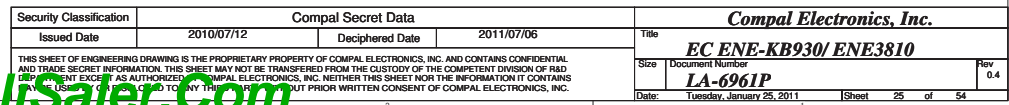
# 10 Board CONN



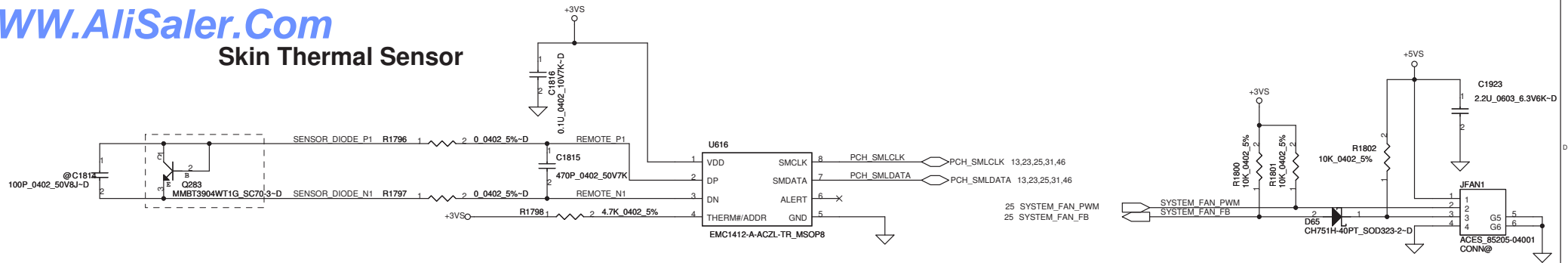
OE#	Function
L	Dect charger
H	D=1D



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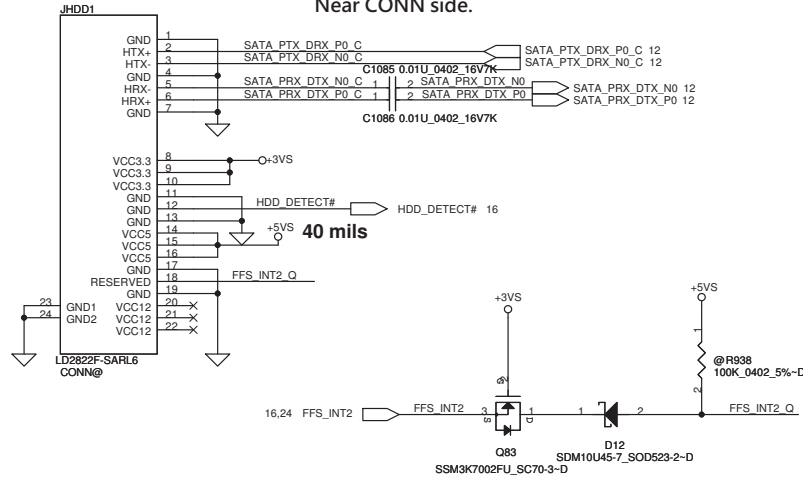


# Skin Thermal Sensor

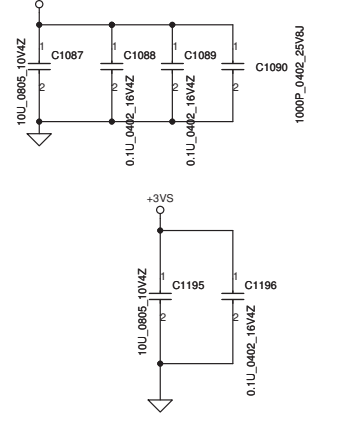


## HDD Connector

Near CONN side.



### Place near HDD CONN (JHDD1)

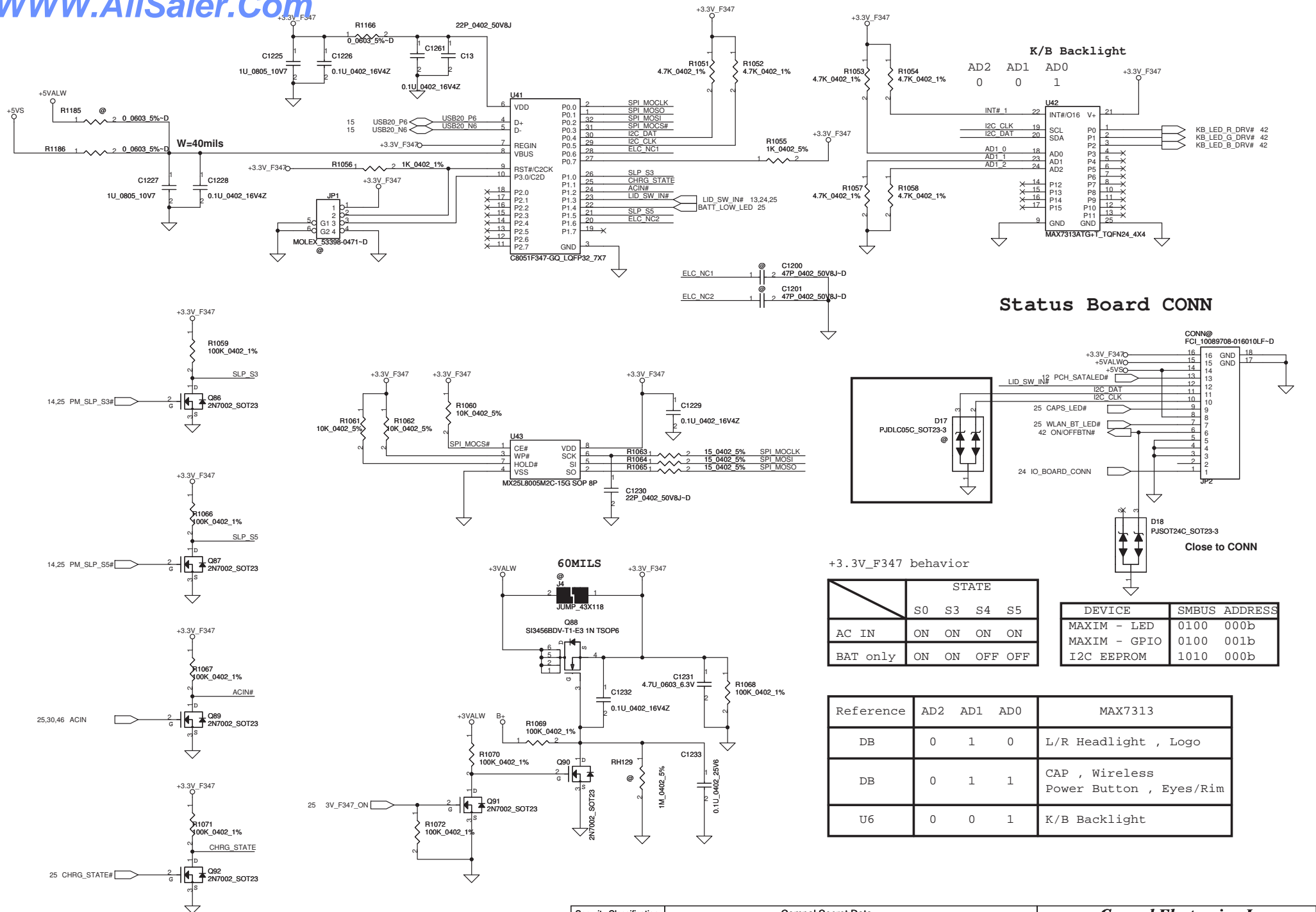


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FAN & Thermal Sensor			
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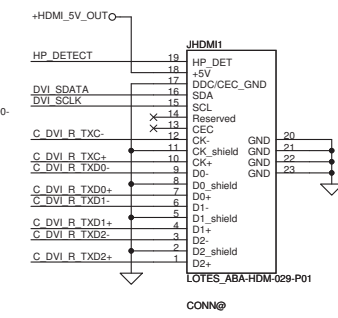
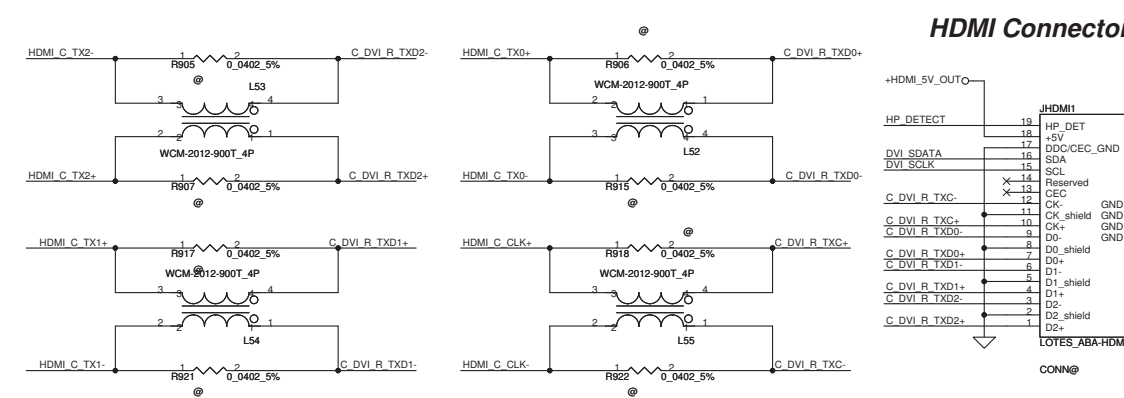
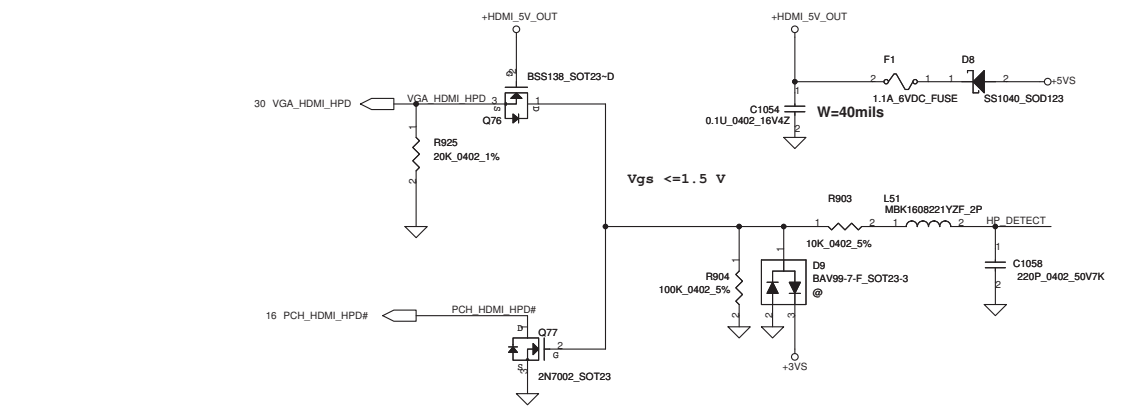
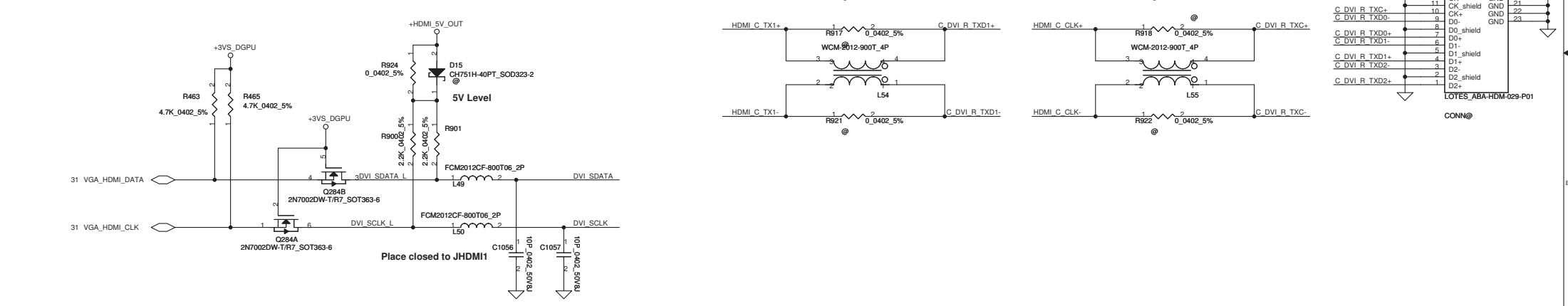
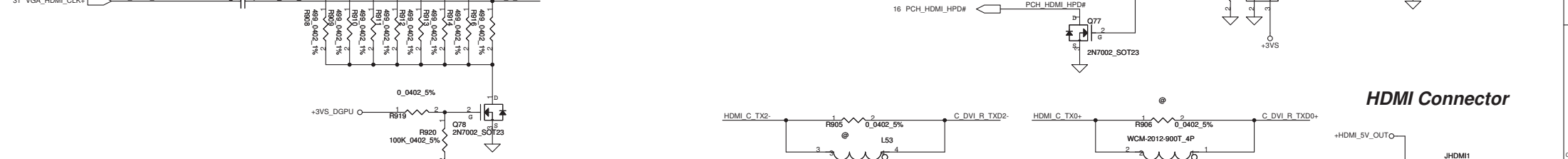


+3.3V\_F347 behavior

	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

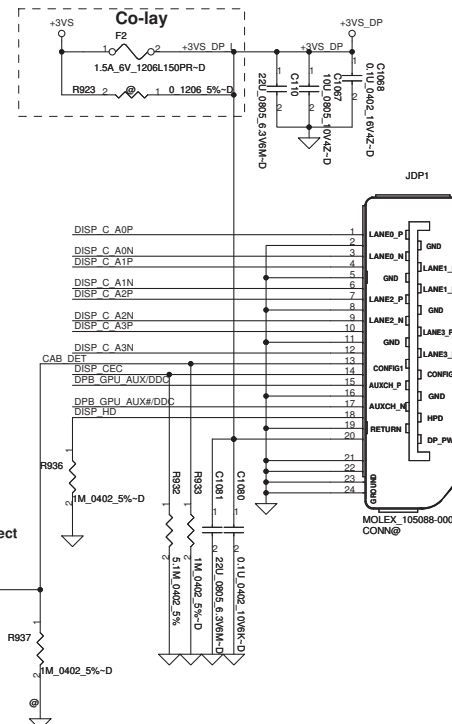
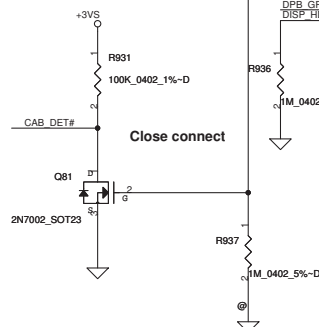
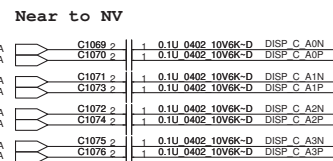
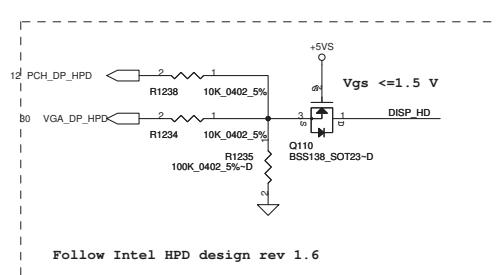
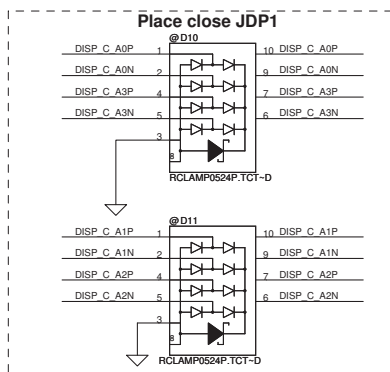
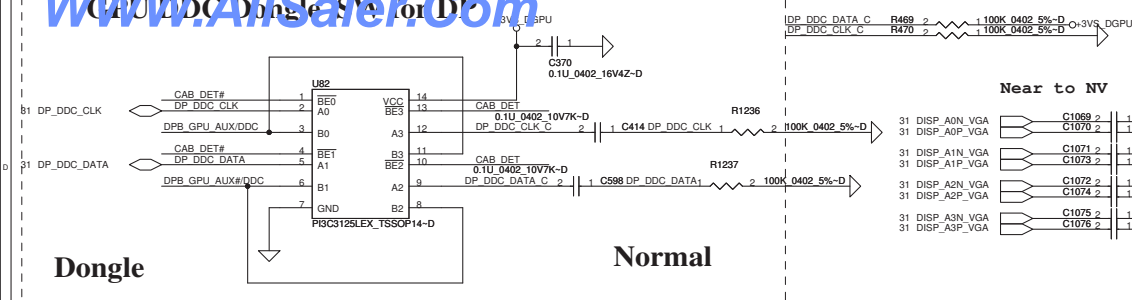
DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

Reference	AD2	AD1	AD0	MAX7313
DB	0	1	0	L/R Headlight , Logo
DB	0	1	1	CAP , Wireless Power Button , Eyes/Rim
U6	0	0	1	K/B Backlight



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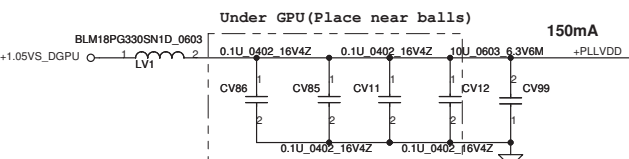
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Date:										Monday, January 24, 2011										Sheet		28		of		54								



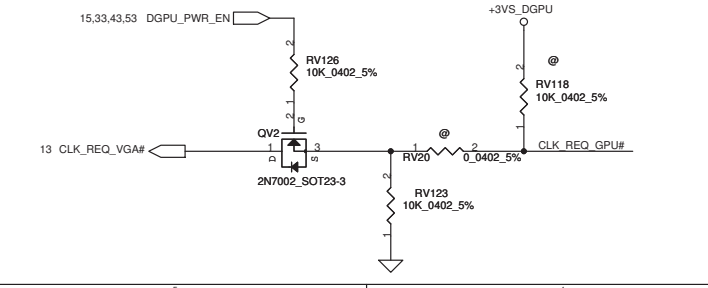
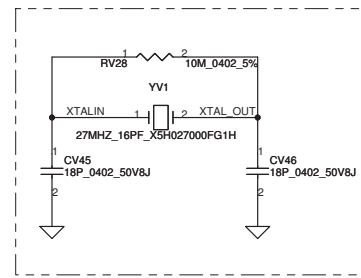
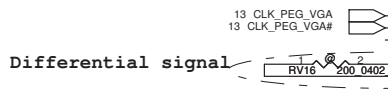
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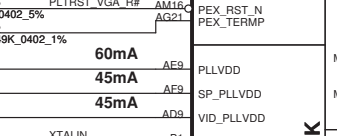
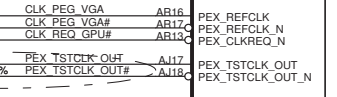


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PEG GTX C HRX P14	CV41	1	2	0.1U_0402_10V7K-D	PEG GTX CRX N14	AL31
PEG GTX C HRX N14	CV42	1	2	0.1U_0402_10V7K-D	PEG GTX CRX P14	AN31
PEG GTX C HRX P15	CV43	1	2	0.1U_0402_10V7K-D	PEG GTX CRX N15	AM32
PEG GTX C HRX N15	CV44	1	2	0.1U_0402_10V7K-D	PEG GTX CRX P15	AN32



PEG HTX C GRX P0	AP17
PEG HTX C GRX N0	AN17
PEG HTX C GRX P1	AP18
PEG HTX C GRX N1	AN18
PEG HTX C GRX P2	AP19
PEG HTX C GRX N2	AN19
PEG HTX C GRX P3	AP20
PEG HTX C GRX N3	AN20
PEG HTX C GRX P4	AP21
PEG HTX C GRX N4	AN21
PEG HTX C GRX P5	AP22
PEG HTX C GRX N5	AN22
PEG HTX C GRX P6	AP23
PEG HTX C GRX N6	AN23
PEG HTX C GRX P7	AP24
PEG HTX C GRX N7	AN24
PEG HTX C GRX P8	AP25
PEG HTX C GRX N8	AN25
PEG HTX C GRX P9	AP26
PEG HTX C GRX N9	AN26
PEG HTX C GRX P10	AP27
PEG HTX C GRX N10	AN27
PEG HTX C GRX P11	AP28
PEG HTX C GRX N11	AN28
PEG HTX C GRX P12	AP29
PEG HTX C GRX N12	AN29
PEG HTX C GRX P13	AP30
PEG HTX C GRX N13	AN30
PEG HTX C GRX P14	AP31
PEG HTX C GRX N14	AN31
PEG HTX C GRX P15	AP32
PEG HTX C GRX N15	AN32

PEG GTX CRX P0	AL17
PEG GTX CRX N0	AN17
PEG GTX CRX P1	AM17
PEG GTX CRX N1	AN17
PEG GTX CRX P2	AL19
PEG GTX CRX N2	AN19
PEG GTX CRX P3	AM20
PEG GTX CRX N3	AN20
PEG GTX CRX P4	AM21
PEG GTX CRX N4	AN21
PEG GTX CRX P5	AM22
PEG GTX CRX N5	AN22
PEG GTX CRX P6	AL23
PEG GTX CRX N6	AN23
PEG GTX CRX P7	AM24
PEG GTX CRX N7	AN24
PEG GTX CRX P8	AL25
PEG GTX CRX N8	AN25
PEG GTX CRX P9	AM26
PEG GTX CRX N9	AN26
PEG GTX CRX P10	AM27
PEG GTX CRX N10	AN27
PEG GTX CRX P11	AM28
PEG GTX CRX N11	AN28
PEG GTX CRX P12	AL29
PEG GTX CRX N12	AN29
PEG GTX CRX P13	AM29
PEG GTX CRX N13	AN29
PEG GTX CRX P14	AM30
PEG GTX CRX N14	AN30
PEG GTX CRX P15	AM31
PEG GTX CRX N15	AN31



XTALIN	R1
XTAL OUT	B2
XTALOUT	D1
XTALSSIN	D2
XTALIN	R1
XTAL OUT	B2
XTALOUT	D1
XTALSSIN	D2
XTALIN	R1
XTAL OUT	B2
XTALOUT	D1
XTALSSIN	D2

N12P-GV1-A1\_BGA\_973P

GPIO0	K1
GPIO1	K2
GPIO2	K3
GPIO3	K4
GPIO4	K5
GPIO5	K6
GPIO6	K7
GPIO7	K8
GPIO8	K9
GPIO9	K10
GPIO10	K11
GPIO11	K12
GPIO12	K13
GPIO13	K14
GPIO14	K15
GPIO15	K16
GPIO16	K17
GPIO17	K18
GPIO18	K19
GPIO19	K20
GPIO20	K21
GPIO21	K22
GPIO22	K23
GPIO23	K24
GPIO24	K25

MIOA_D0_NC	N1
MIOA_D1_NC	N2
MIOA_D2_NC	N3
MIOA_D3_NC	N4
MIOA_D4_NC	N5
MIOA_D5_NC	N6
MIOA_D6_NC	N7
MIOA_D7_NC	N8
MIOA_D8_NC	N9
MIOA_D9_NC	N10
MIOA_D10_NC	N11
MIOA_D11_NC	N12
MIOA_D12_NC	N13
MIOA_D13_NC	N14
MIOA_D14_NC	N15
MIOB_D0_NC	N16
MIOB_D1_NC	N17
MIOB_D2_NC	N18
MIOB_D3_NC	N19
MIOB_D4_NC	N20
MIOB_D5_NC	N21
MIOB_D6_NC	N22
MIOB_D7_NC	N23
MIOB_D8_NC	N24
MIOB_D9_NC	N25
MIOB_D10_NC	N26
MIOB_D11_NC	N27
MIOB_D12_NC	N28
MIOB_D13_NC	N29
MIOB_D14_NC	N30

MIOA_DE_NC	N2
MIOA_CTL3_NC	N3
MIOA_VREF_NC	N4
MIOB_DE_NC	N5
MIOB_CTL3_NC	N6
MIOB_VREF_NC	N7

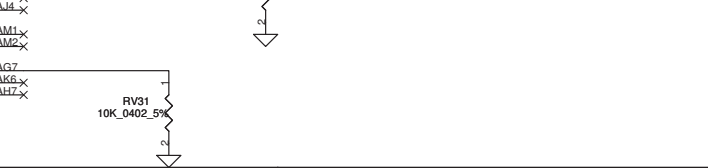
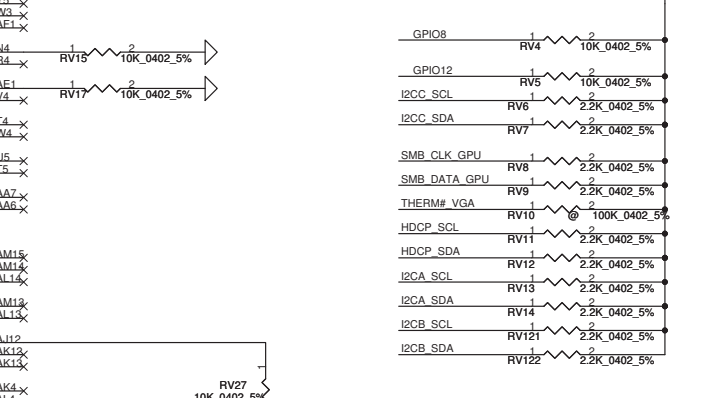
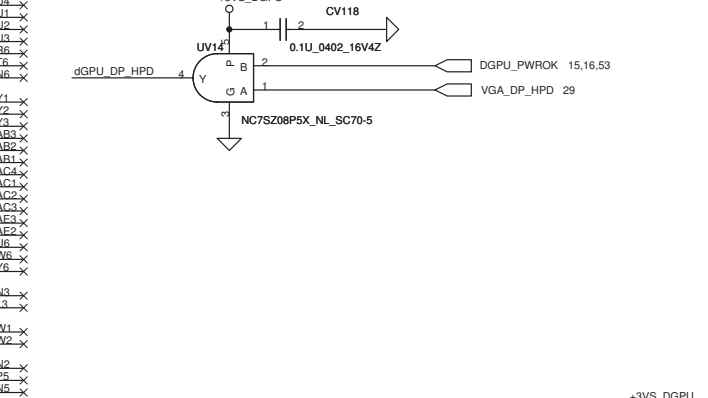
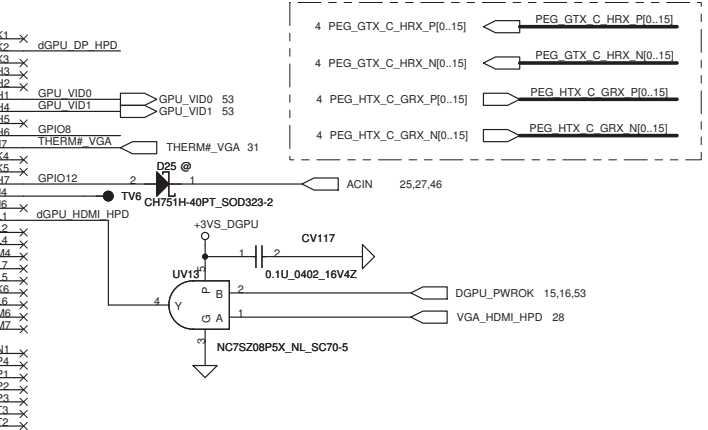
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MIOA_CLKOUT_NC	N9
MIOB_CLKIN_NC	N10
MIOB_CLKOUT_NC	N11
MIOA_CLKOUT_NC	N12
MIOB_CLKOUT_NC	N13

MIOACAL_PD_VDDQ_NC	N14
MIOACAL_PD_GND_NC	N15
MIOBCAL_PD_VDDQ_NC	N16
MIOBCAL_PD_GND_NC	N17

DACA_RED	N18
DACA_GREEN	N19
DACA_BLUE	N20
DACA_HSYNC	N21
DACA_VSYNC	N22

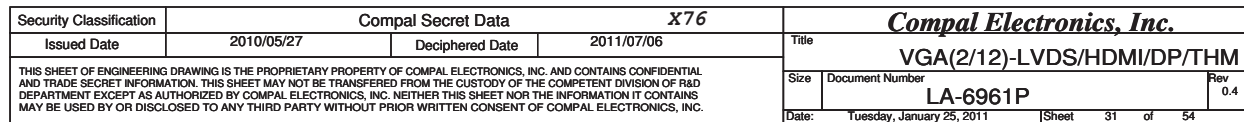
DACB_RED	N23
DACB_GREEN	N24
DACB_BLUE	N25
DACB_HSYNC	N26
DACB_VSYNC	N27

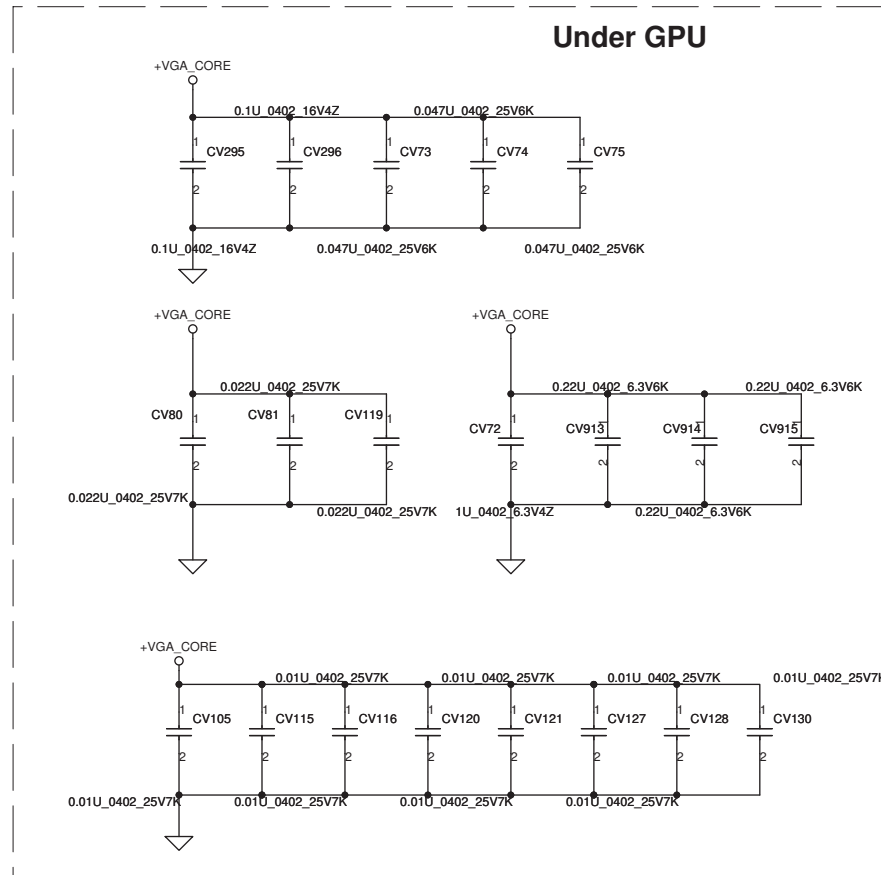
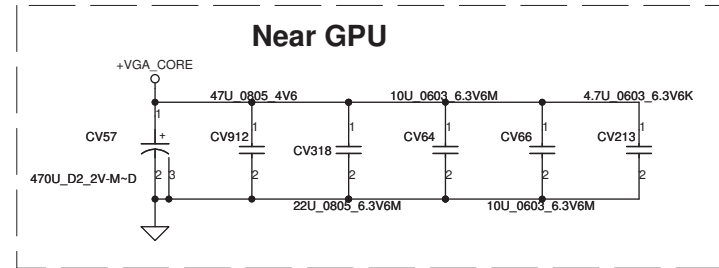
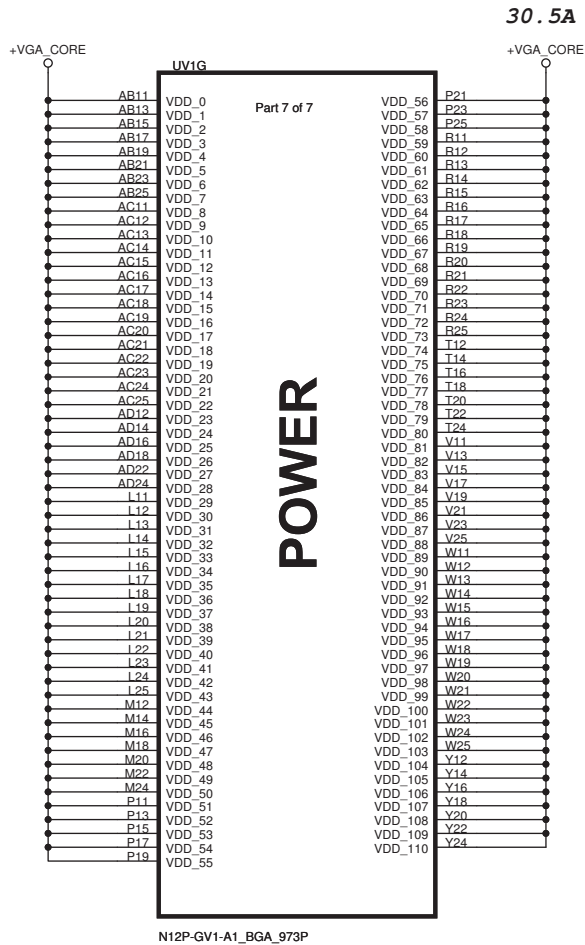
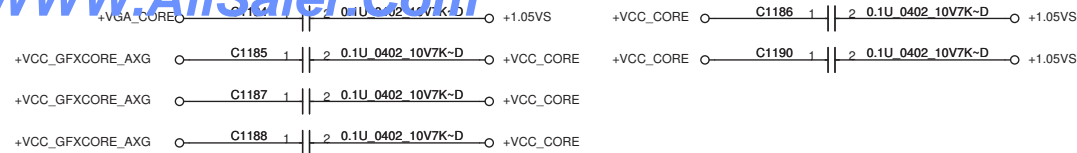
DACB_VDD	N28
DACB_VREF	N29
DACB_RSET	N30



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D

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C

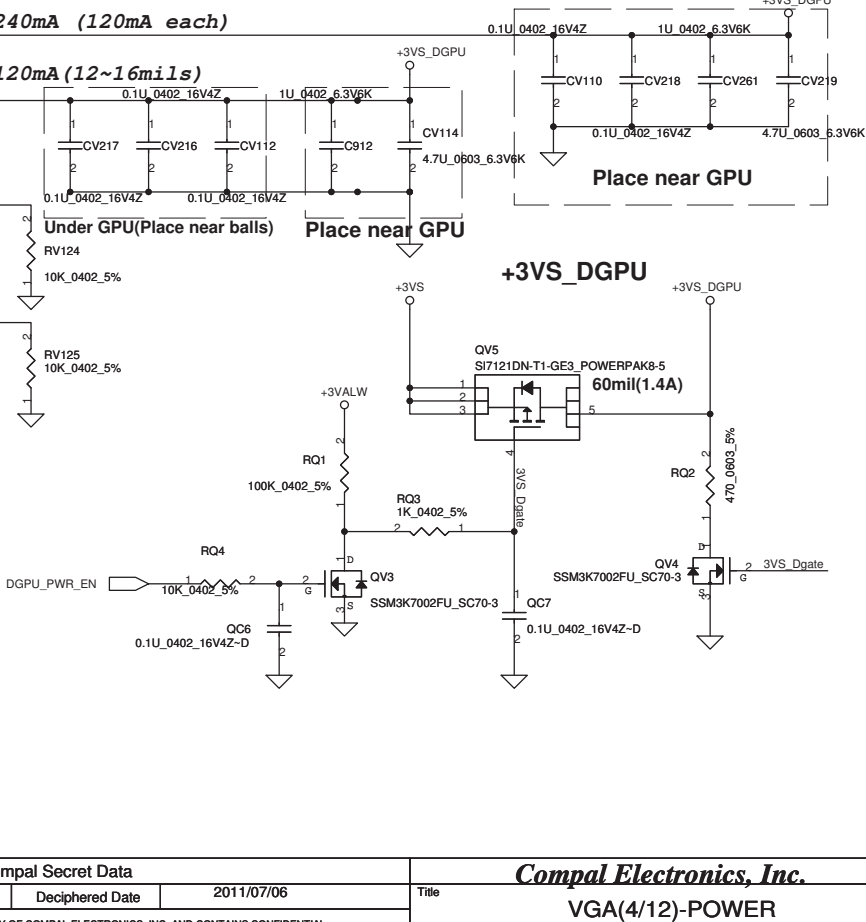
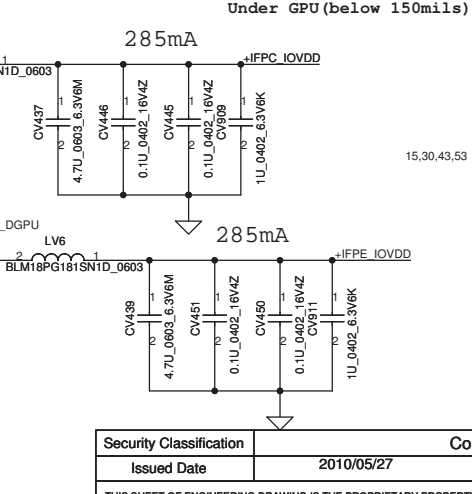
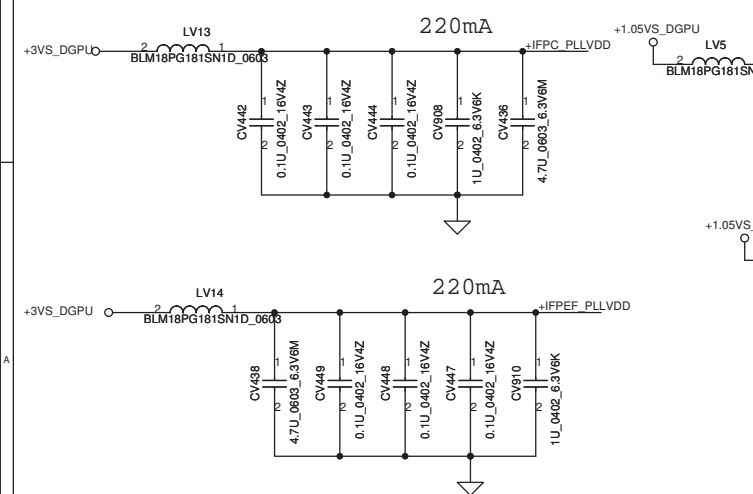
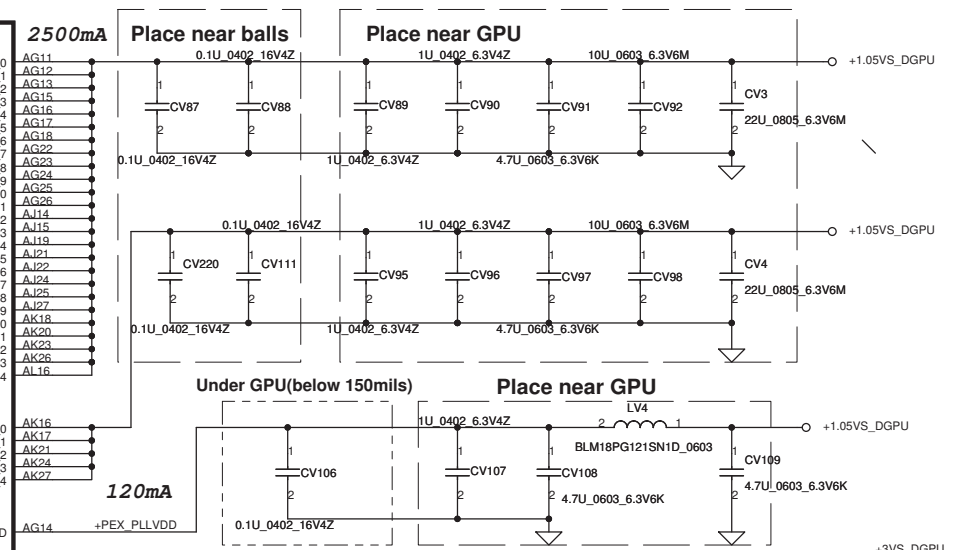
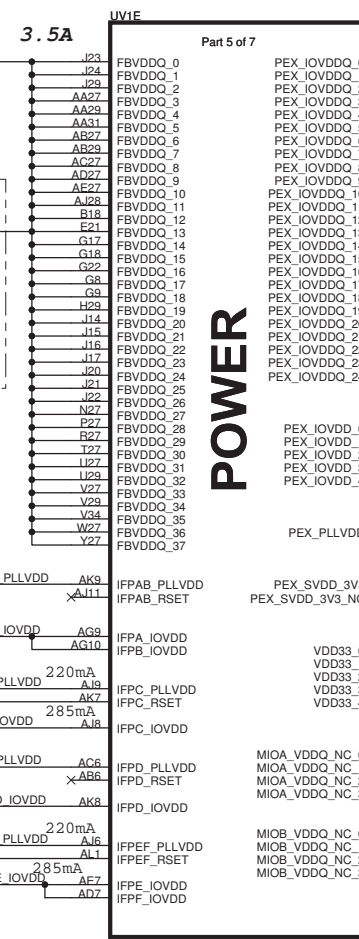
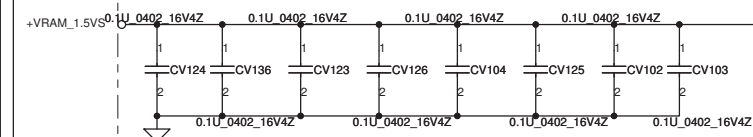
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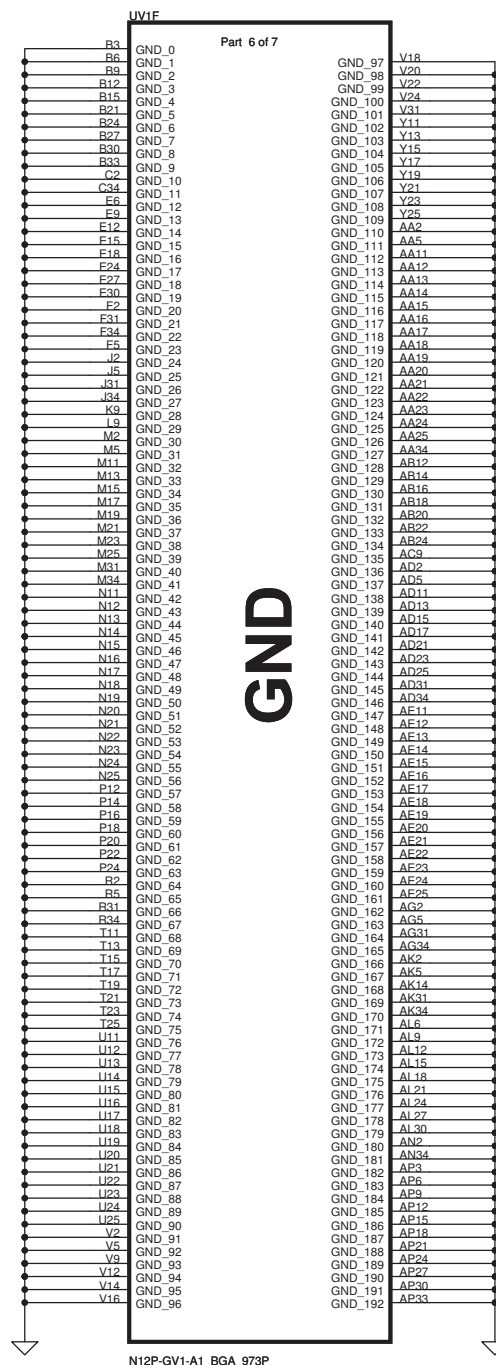
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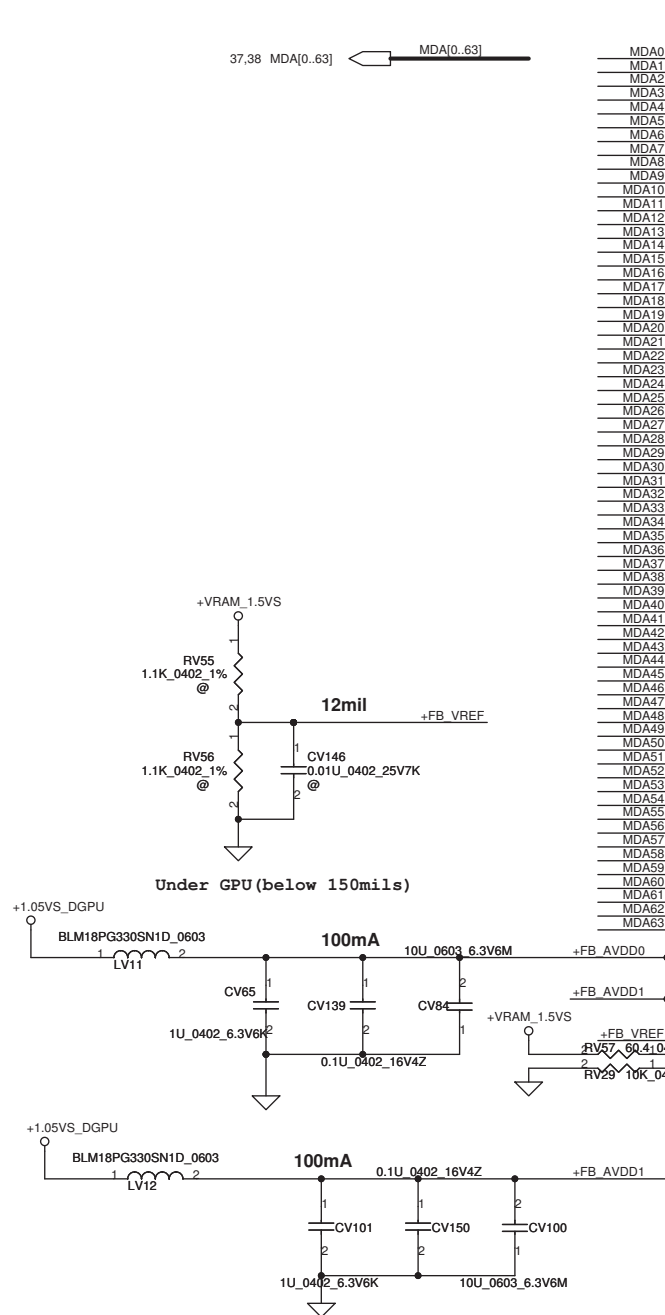


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UV1B

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MDA0 I-32 FBA D0

MDA1 N33 FBA D1

MDA2 L33 FBA D2

MDA3 N34 FBA D3

MDA4 P35 FBA D4

MDA5 P35 FBA D5

MDA6 P33 FBA D6

MDA7 P34 FBA D7

MDA8 K35 FBA D8

MDA9 K33 FBA D9

MDA10 K34 FBA D10

MDA11 H33 FBA D11

MDA12 G34 FBA D12

MDA13 Q33 FBA D13

MDA14 F34 FBA D14

MDA15 F33 FBA D15

MDA16 G31 FBA D16

MDA17 F30 FBA D17

MDA18 G30 FBA D18

MDA19 G32 FBA D19

MDA20 K30 FBA D20

MDA21 K32 FBA D21

MDA22 H30 FBA D22

MDA23 K31 FBA D23

MDA24 L31 FBA D24

MDA25 L30 FBA D25

MDA26 M32 FBA D26

MDA27 N30 FBA D27

MDA28 M30 FBA D28

MDA29 P31 FBA D29

MDA30 R32 FBA D30

MDA31 R30 FBA D31

MDA32 AG30 FBA D32

MDA33 AG32 FBA D33

MDA34 AH31 FBA D34

MDA35 AE31 FBA D35

MDA36 AE30 FBA D36

MDA37 AE30 FBA D37

MDA38 AC32 FBA D38

MDA39 AD30 FBA D39

MDA40 AN33 FBA D40

MDA41 AL31 FBA D41

MDA42 AM33 FBA D42

MDA43 AL33 FBA D43

MDA44 AK30 FBA D44

MDA45 AK32 FBA D45

MDA46 AJ30 FBA D46

MDA47 AH30 FBA D47

MDA48 AH33 FBA D48

MDA49 AH35 FBA D49

MDA50 AH34 FBA D50

MDA51 AH32 FBA D51

MDA52 AJ33 FBA D52

MDA53 AI35 FBA D53

MDA54 AM34 FBA D54

MDA55 AM35 FBA D55

MDA56 AE33 FBA D56

MDA57 AE32 FBA D57

MDA58 AE35 FBA D58

MDA59 AE34 FBA D59

MDA60 AE34 FBA D60

MDA61 AE33 FBA D61

MDA62 AB32 FBA D62

MDA63 AC35 FBA D63

FBA DQM0 P32 DQMA0

FBA DQM1 H34 DQMA1

FBA DQM2 J30 DQMA2

FBA DQM3 P30 DQMA3

FBA DQM4 AE32 DQMA4

FBA DQM5 AL32 DQMA5

FBA DQM6 AL34 DQMA6

FBA DQM7 AE35 DQMA7

FBA DQS\_RN0 J35 DQSA#0

FBA DQS\_RN1 G35 DQSA#1

FBA DQS\_RN2 H31 DQSA#2

FBA DQS\_RN3 M32 DQSA#3

FBA DQS\_RN4 AD32 DQSA#4

FBA DQS\_RN5 AJ31 DQSA#5

FBA DQS\_RN6 AJ35 DQSA#6

FBA DQS\_RN7 AC34 DQSA#7

FBA DQS\_WP0 L34 DQSA0

FBA DQS\_WP1 H35 DQSA1

FBA DQS\_WP2 J32 DQSA2

FBA DQS\_WP3 N31 DQSA3

FBA DQS\_WP4 AE31 DQSA4

FBA DQS\_WP5 AJ32 DQSA5

FBA DQS\_WP6 AJ34 DQSA6

FBA DQS\_WP7 AC33 DQSA7

FBA WCK0 P29 WCK0\_N

FBA WCK1 L29 WCK1\_N

FBA WCK2 M29 WCK2\_N

FBA WCK3 AH29 WCK3\_N

FBA CLK0 T32 CLKA0

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FBA CLK1 AC30 CLKA1#

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FB\_PLLAVDD\_1 J18

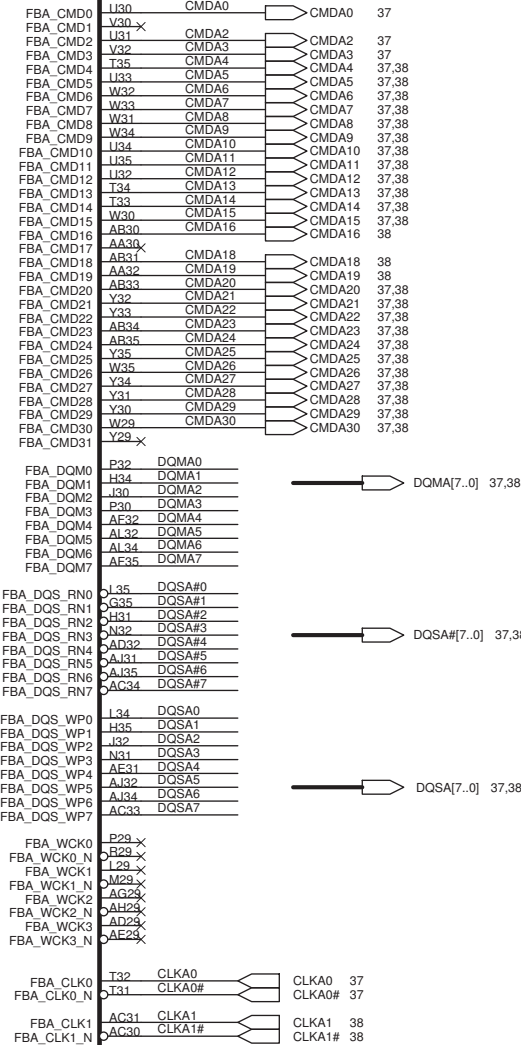
FB\_VREF\_NC J27

FBA\_DEBUG0 T29

FBA\_DEBUG1 T29

N12P-GV1-A1\_BGA\_973P

# MEMORY INTERFACE



## Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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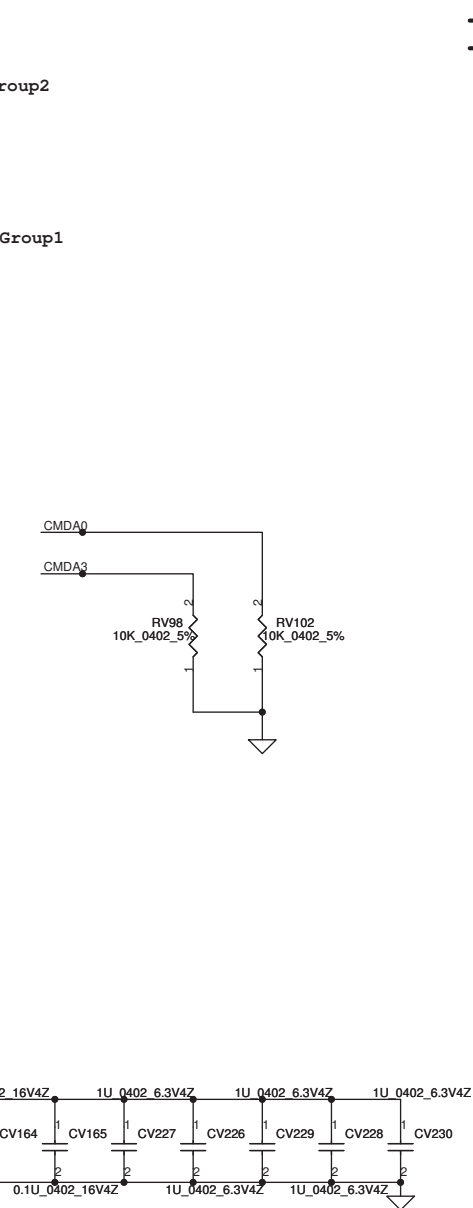
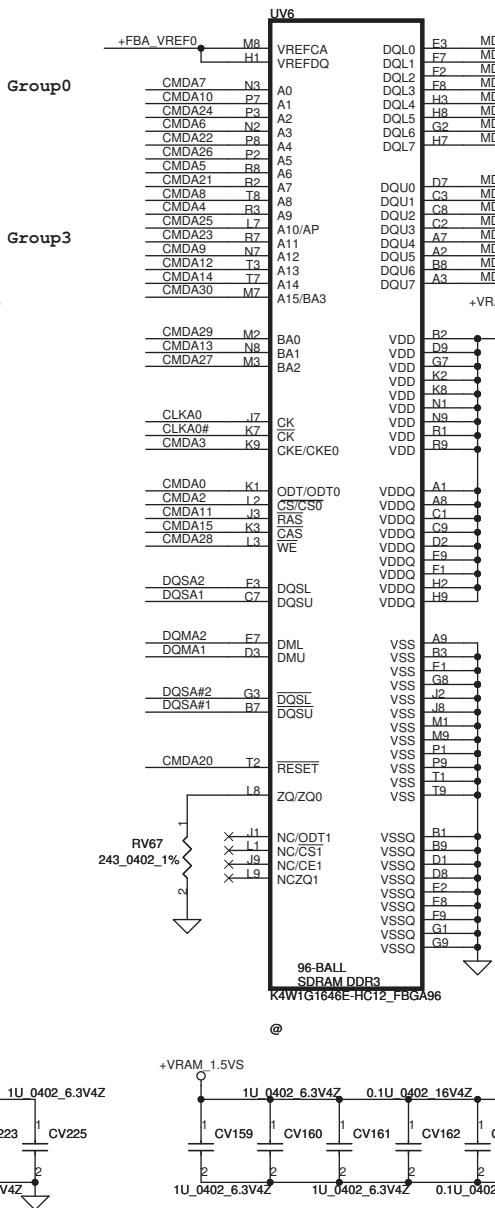
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MDb7	D16	FBC_D7	MDb8	D19	CMDB8	39,40
MDb8	C13	FBC_CMD8	D20	CMDB9	CMDB8	39,40



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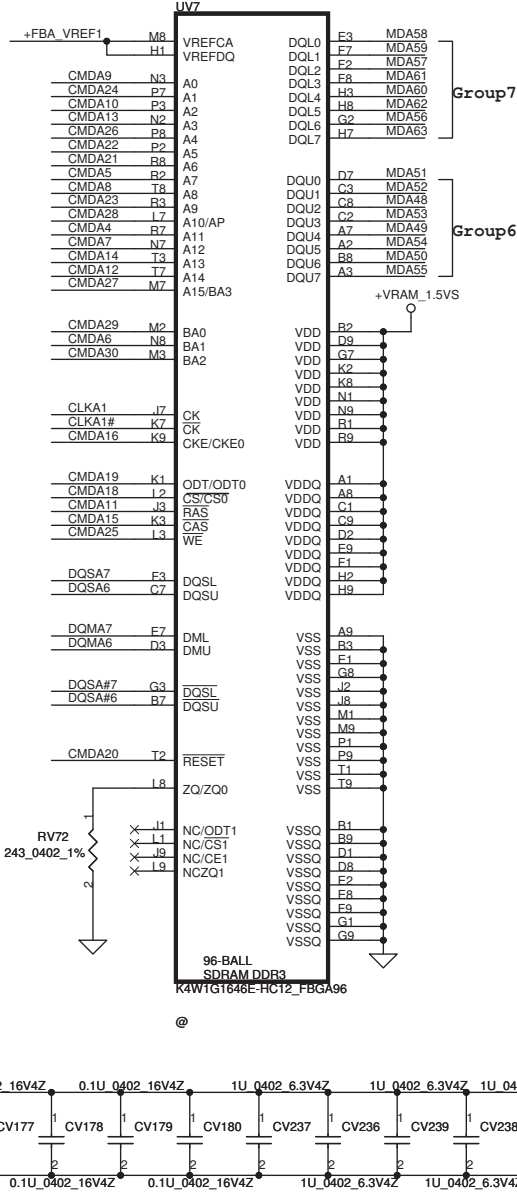
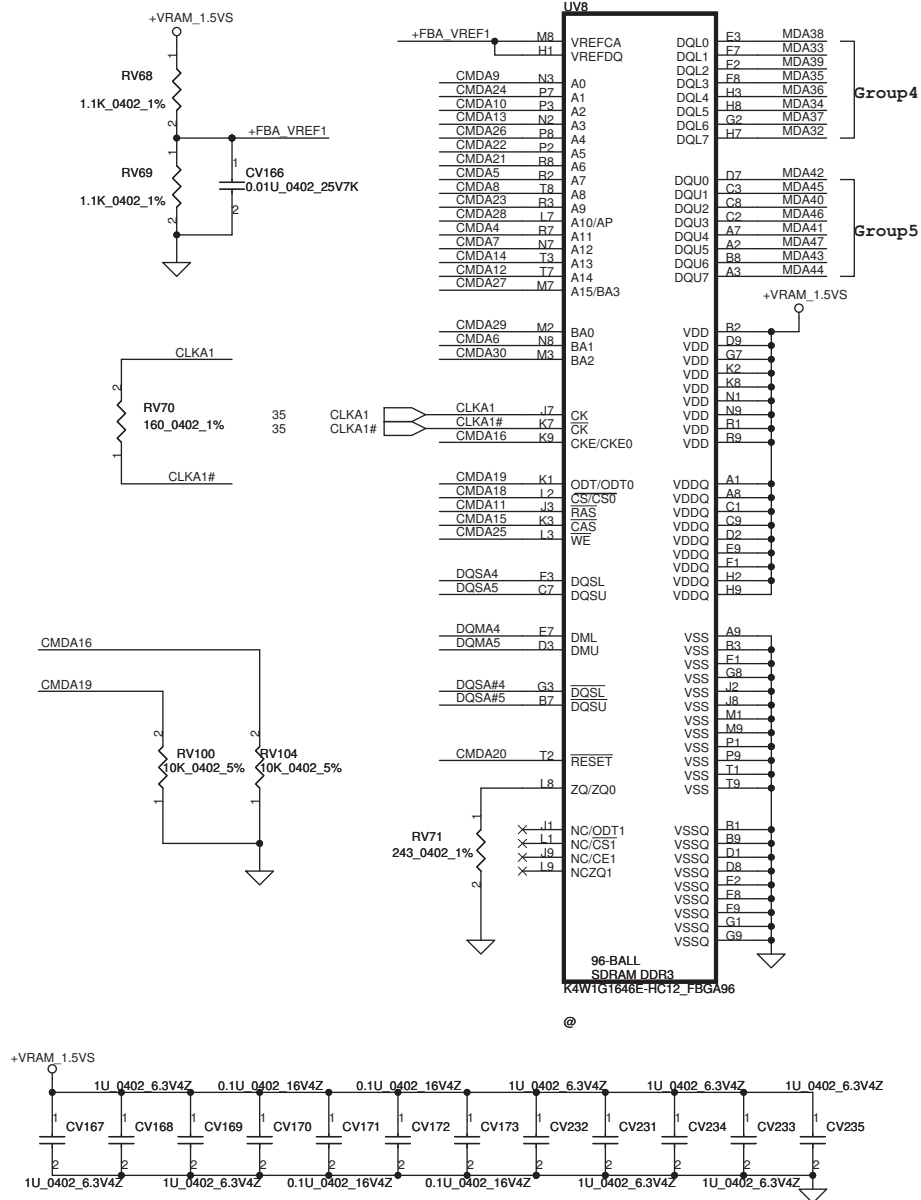




Mode E - Mirror  
Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

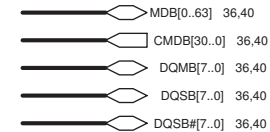
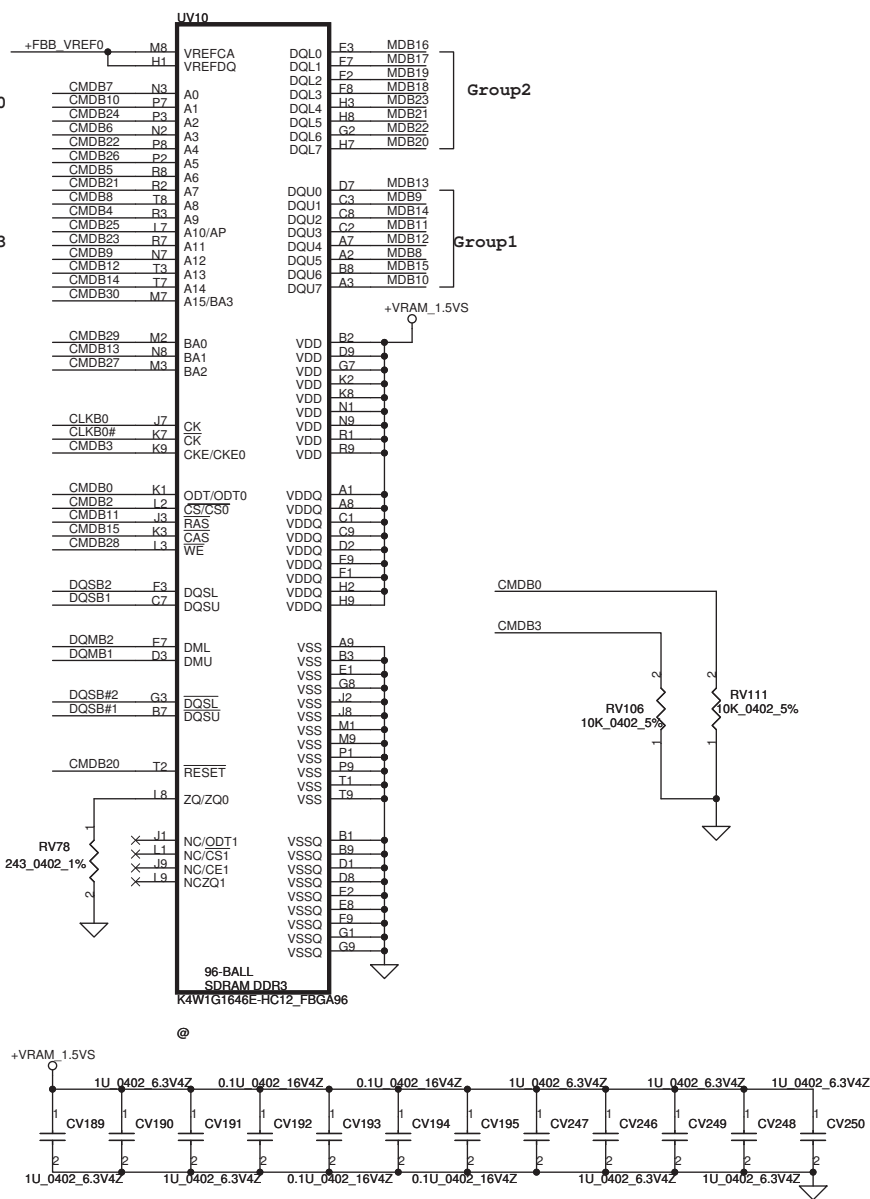
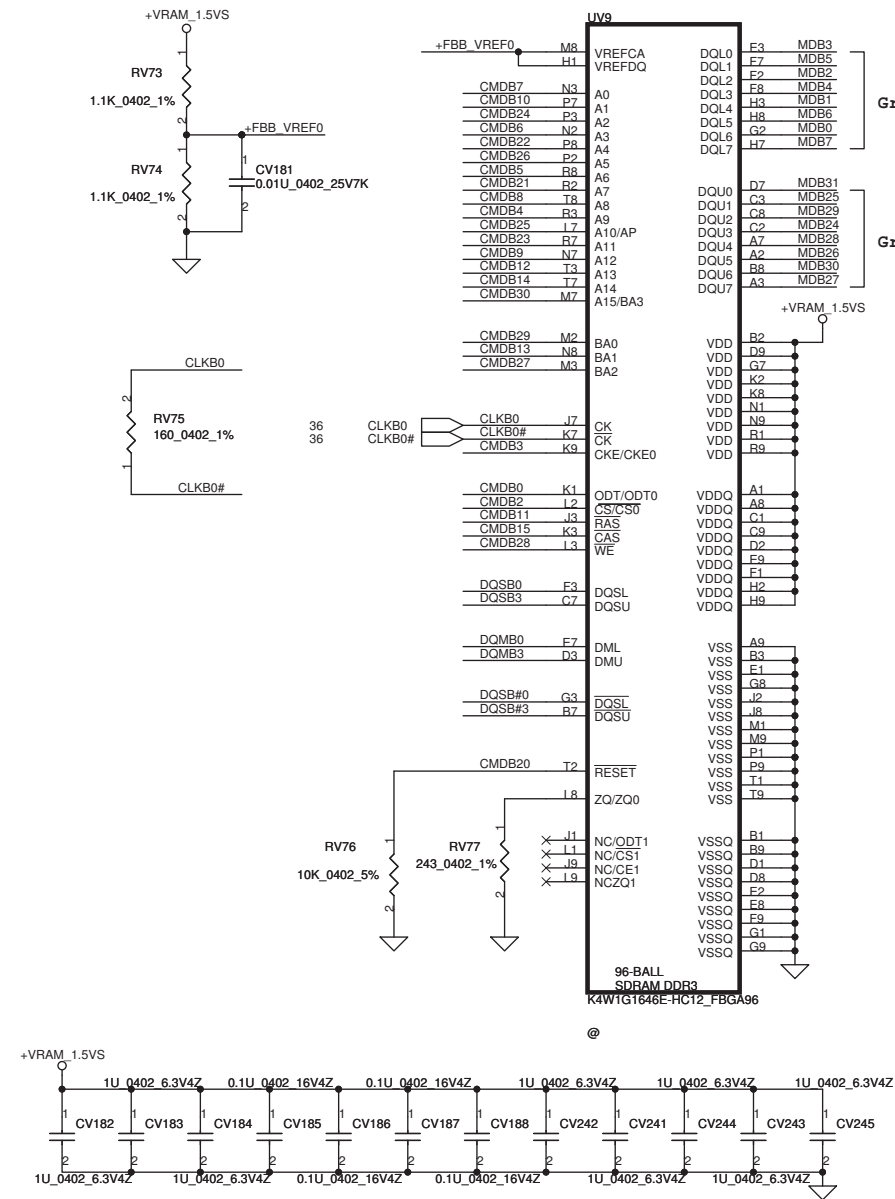
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Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

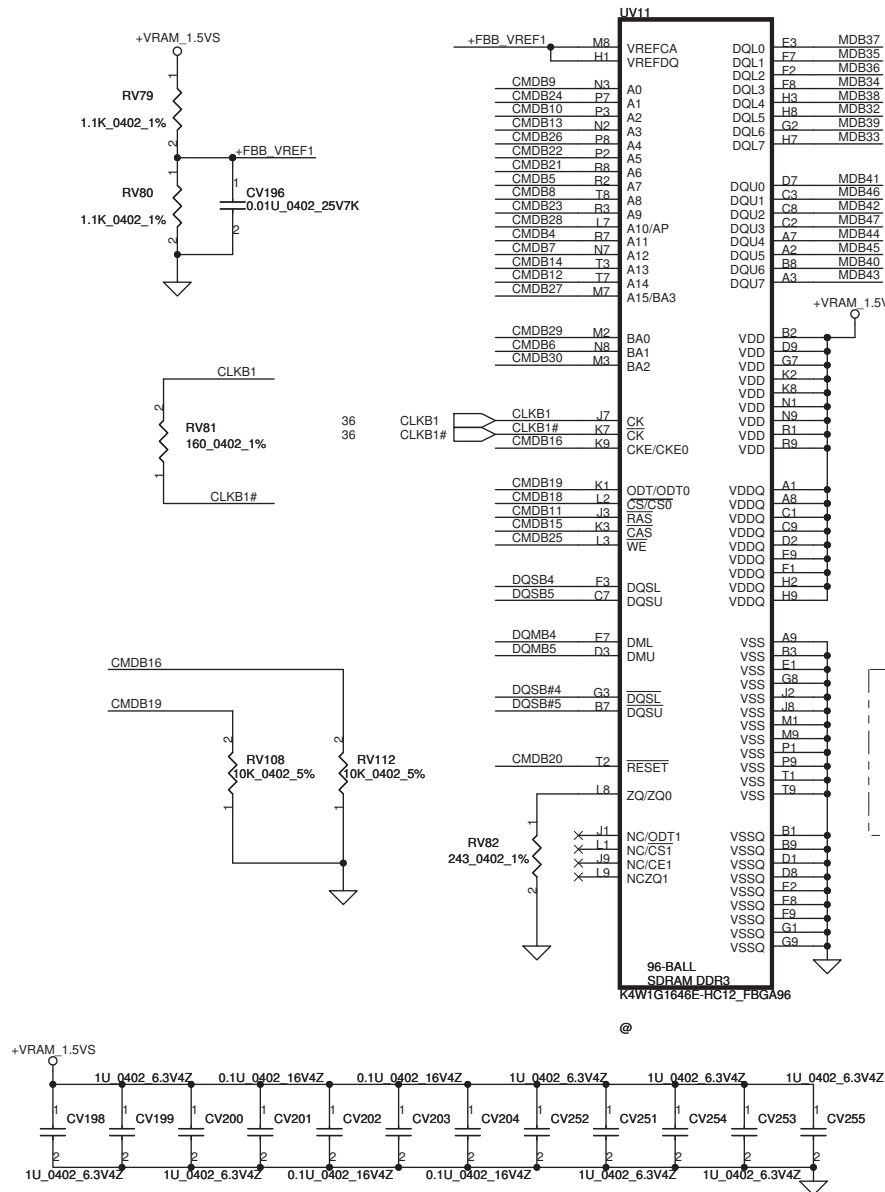
# Memory Partition C - Lower 32 bits



## Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

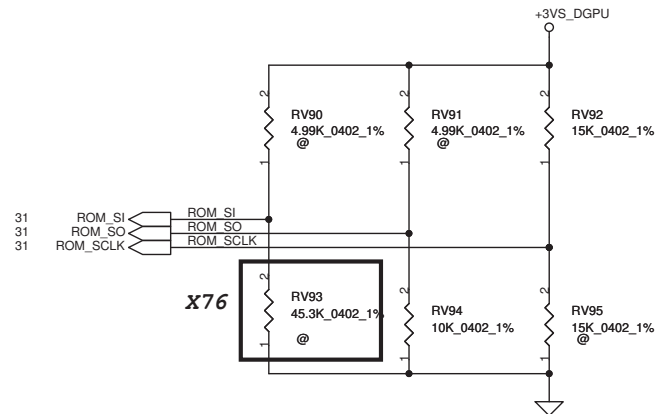
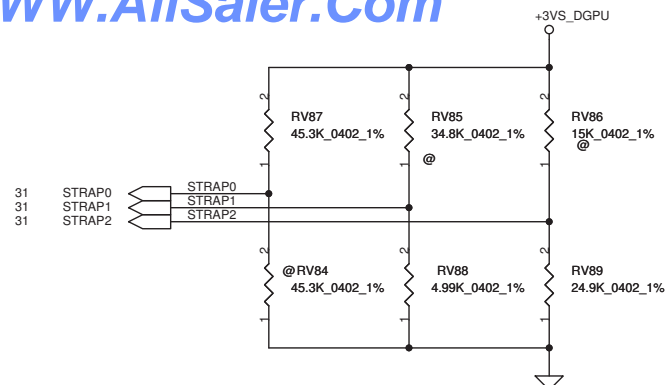
# Memory Partition C - Upper 32 bits



## Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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N12P-GS-A1 :  
 ROM\_SO : PL-10K  
 ROM\_CLK : PH-15K  
 ROM\_SI : PL45.3K (Samsung 2GB)  
 Strap 2 : PL-5K  
 Strap 1 : PH-35K  
 Strap 0 : PH-45K

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S20	1GB	0010	PD 15K (SD034150280)
Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003Y000	2GB	0110	PD 34.8k(SD034348280)
Samsung (900MHZ) 64MX16 K4W1G1646E-HC11 SA000041T00	1GB	0011	PD 20K (SD034200280)
Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q00	2GB	0111	PD 45.3K(SD034453280)

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12M-GE	0x0A7A	Pull up 15K	Pull up 15K
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

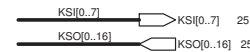
PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

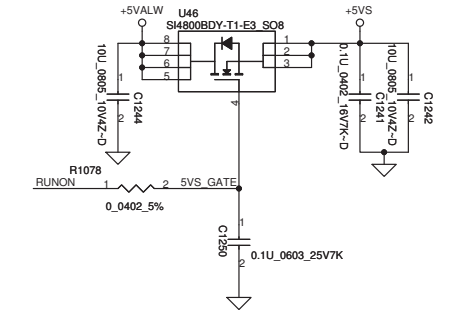
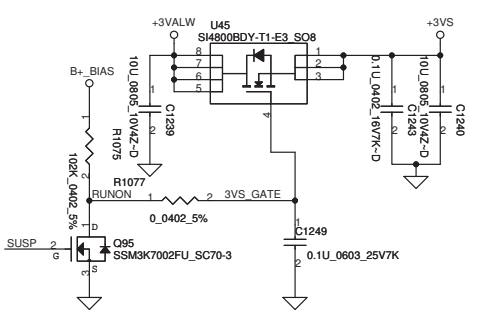
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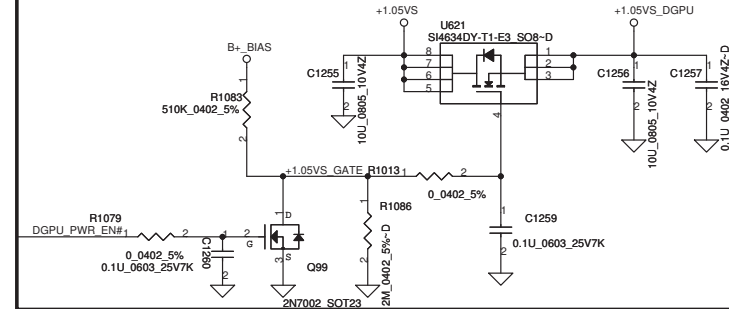
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## +5VALW to +5VS Transfer

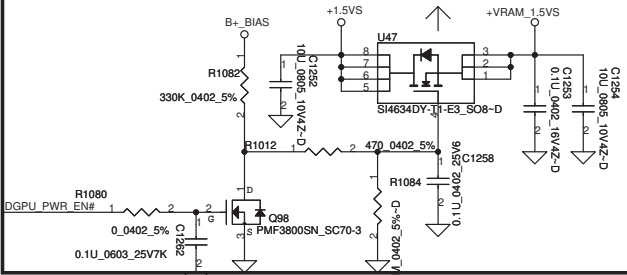


## +1.05V to +1.05VS\_DGPU Transfer

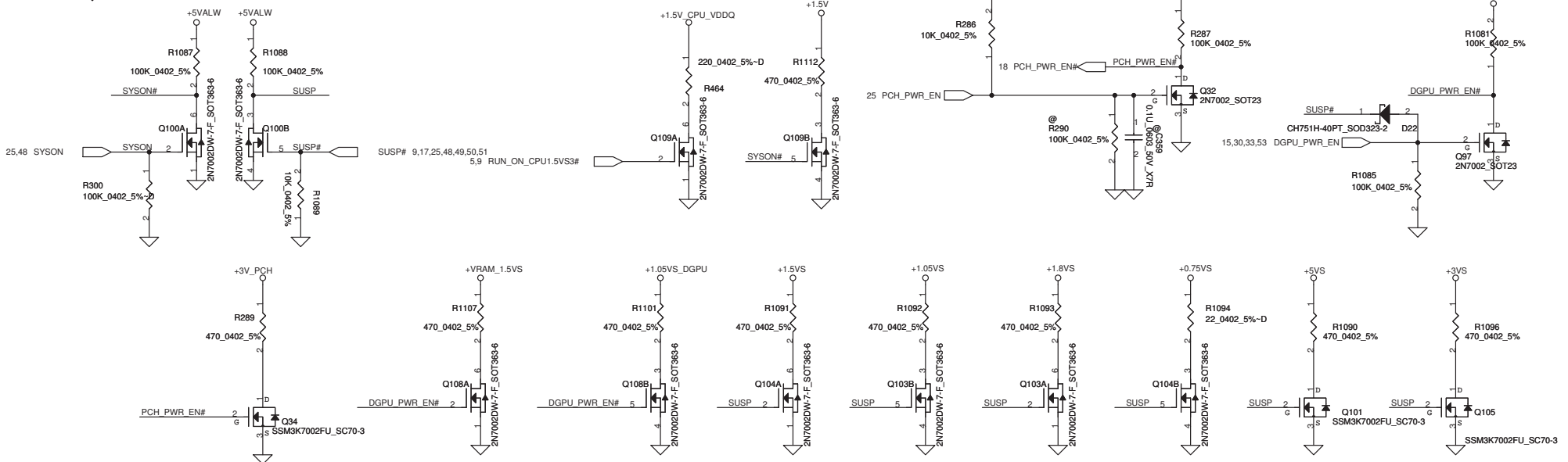
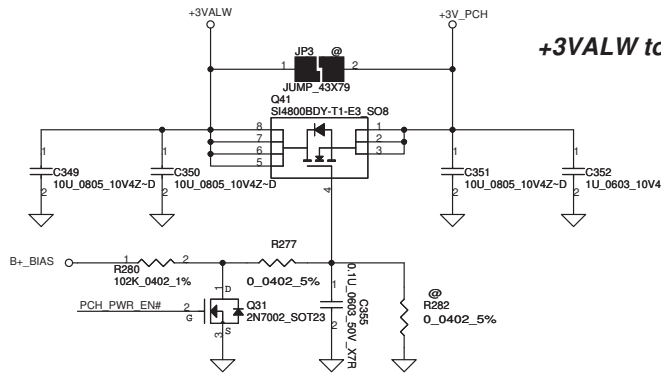


## +1.5VS to +1.5VSDGPU Transfer

SB54392008L EOL, P/N change to SB54800038L

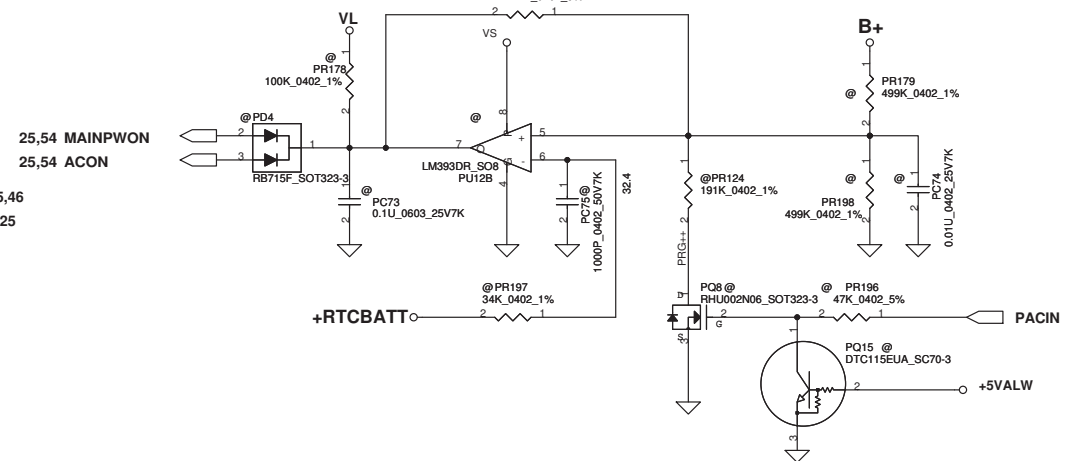
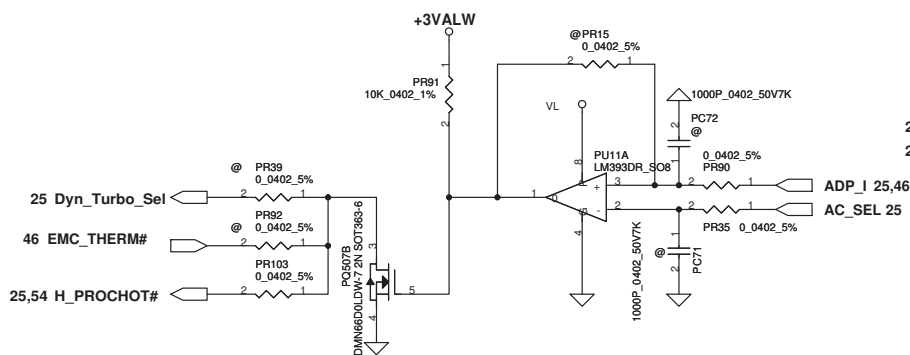
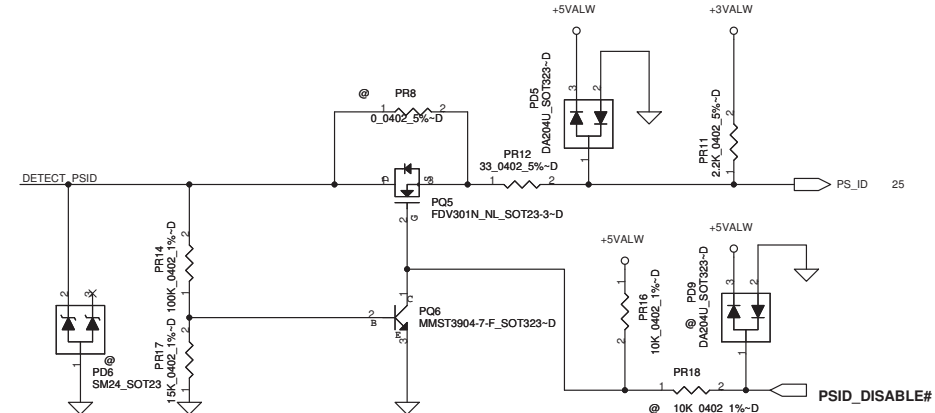
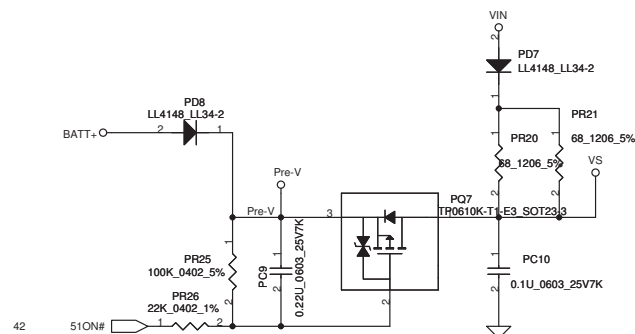
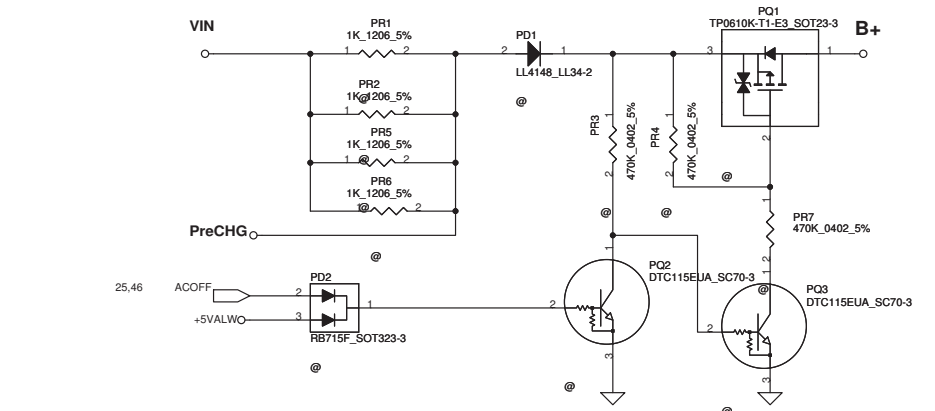
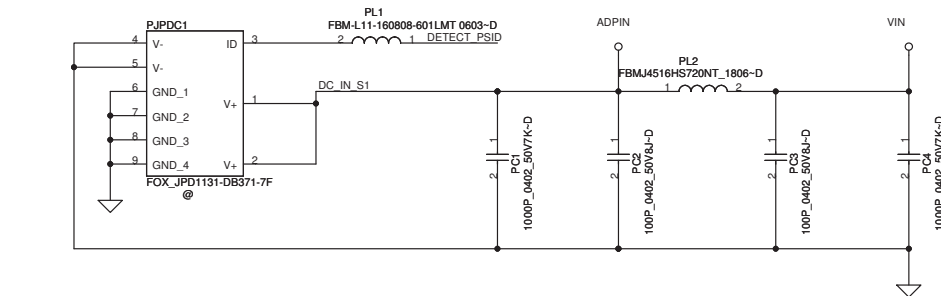


## +3VALW to +3V\_PCH Transfer

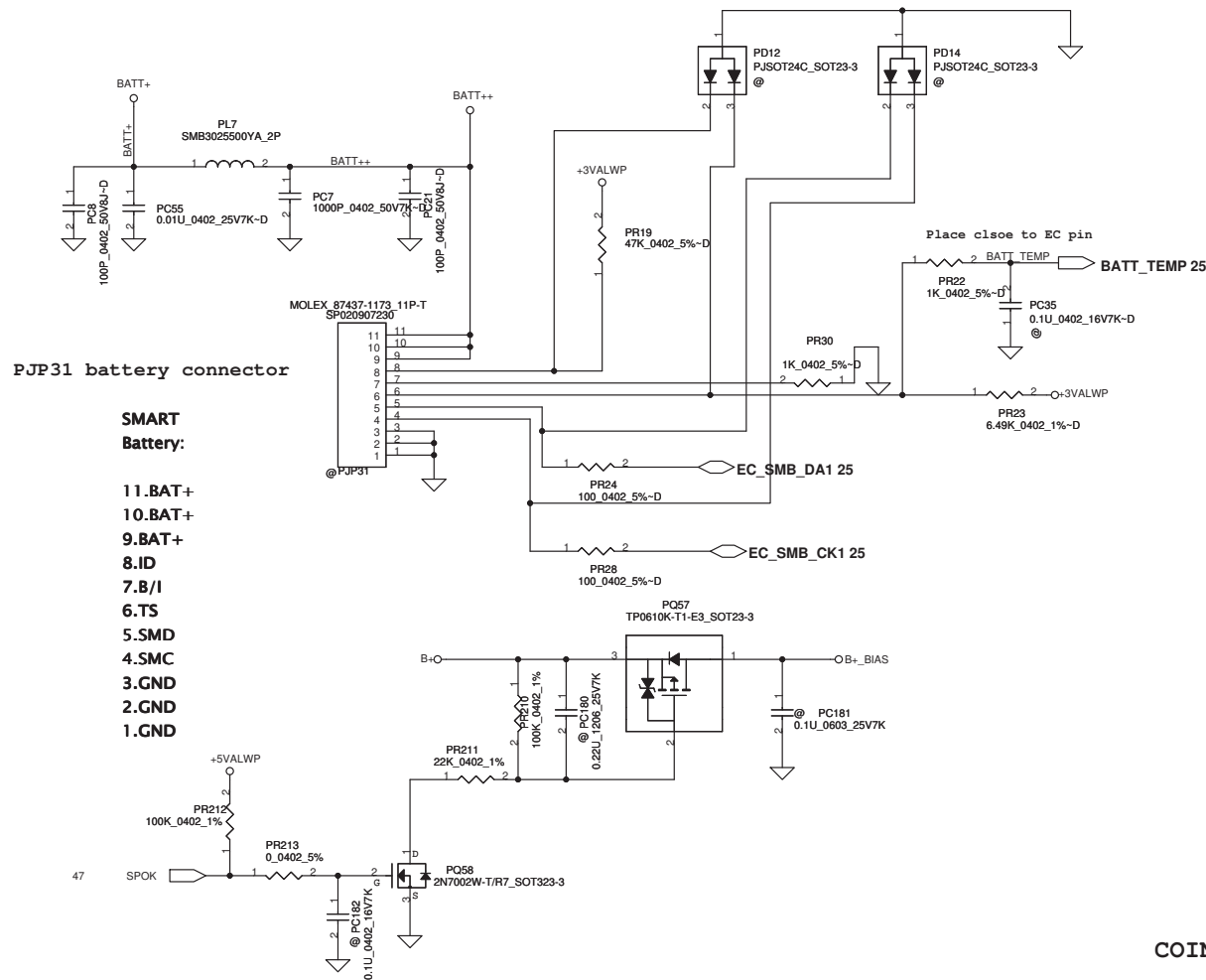


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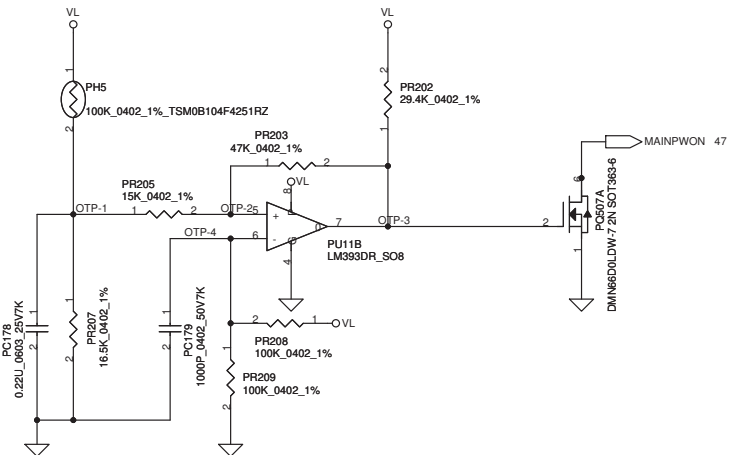


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Issued Date	2009/12/01	Deciphered Date	2010/05/28	PWR-DCIN / Vin Detector	
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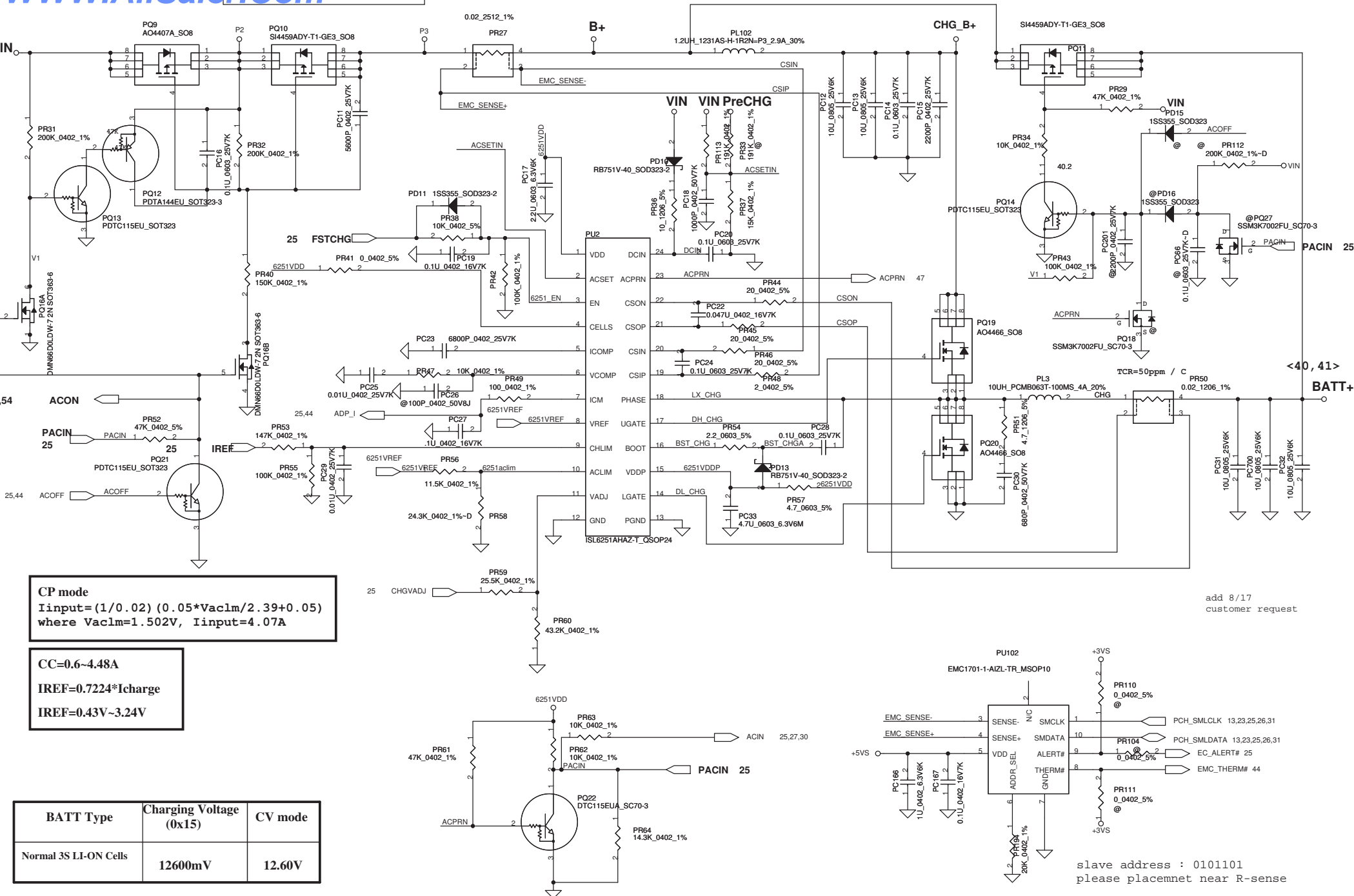


## Battery Connect/OTP

**PH3 under CPU bottom side :**  
CPU thermal protection at 90 degree C  
Recovery at 50 degree C



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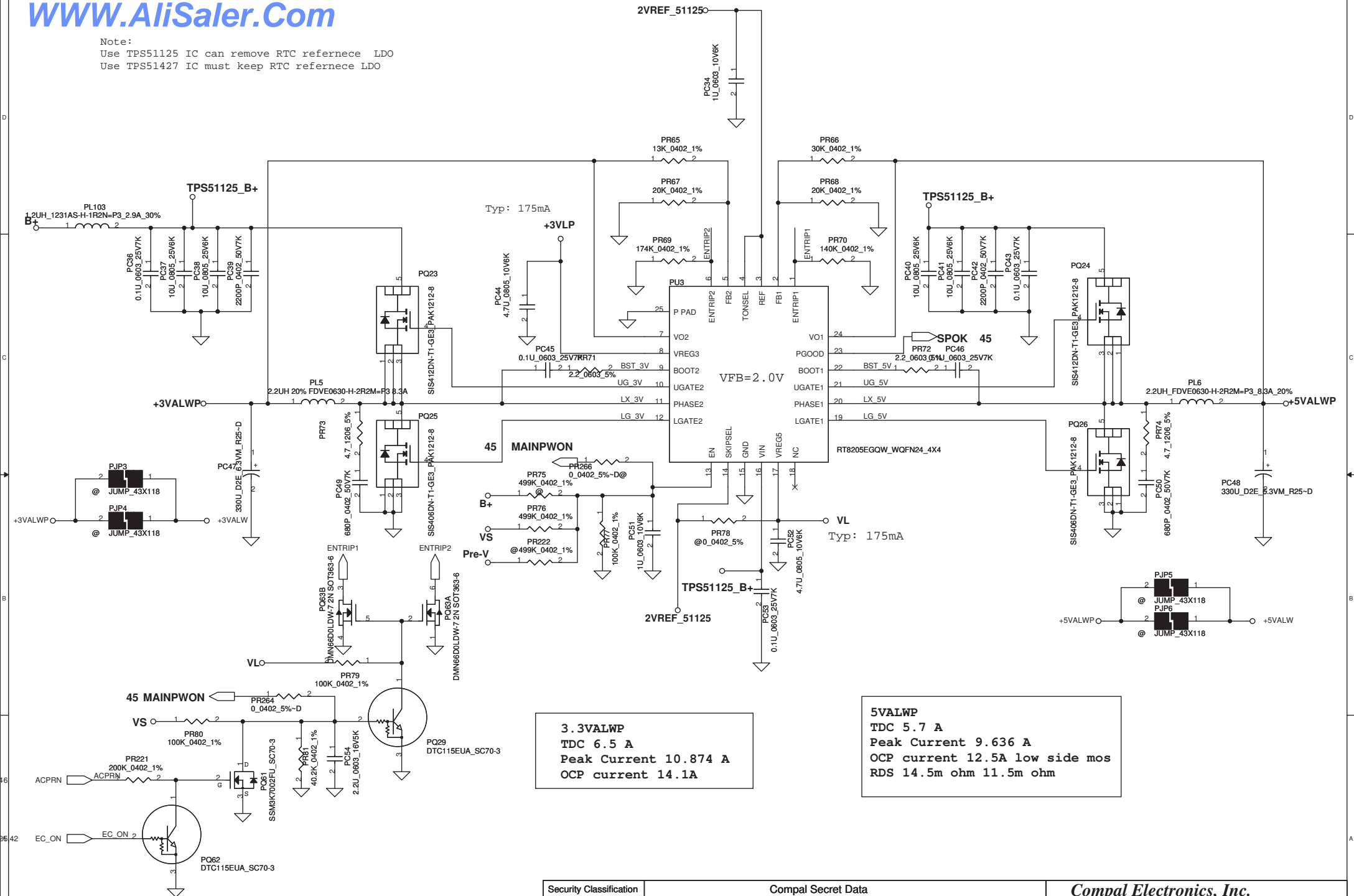


CP mode  
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$   
 where  $V_{ac1m} = 1.502V$ ,  $I_{input} = 4.07A$

CC=0.6-4.48A  
 $I_{REF} = 0.7224 * I_{charge}$   
 $I_{REF} = 0.43V \sim 3.24V$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

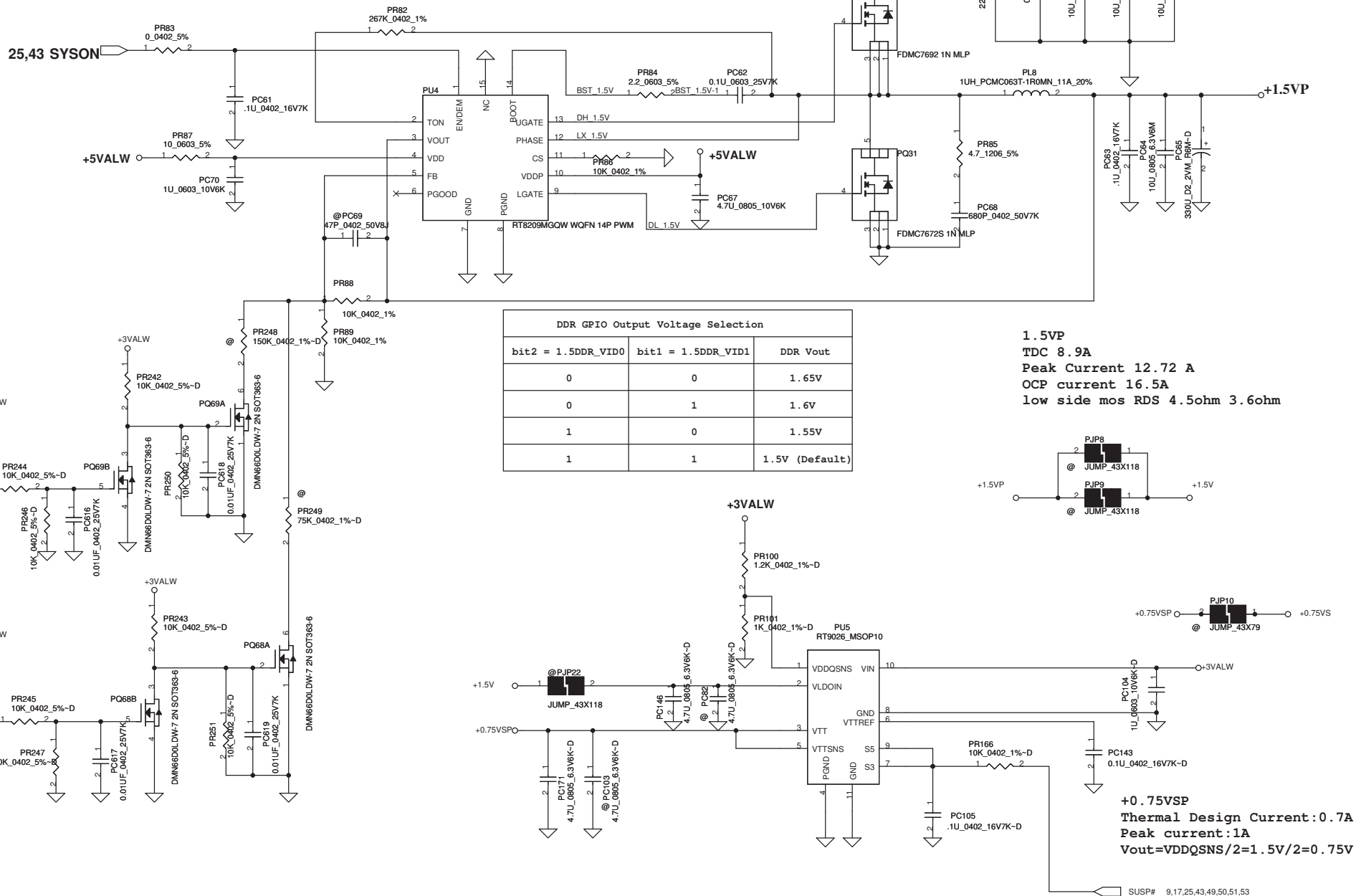
Note:  
Use TPS51125 IC can remove RTC refernece LDO  
Use TPS51427 IC must keep RTC refernece LDO



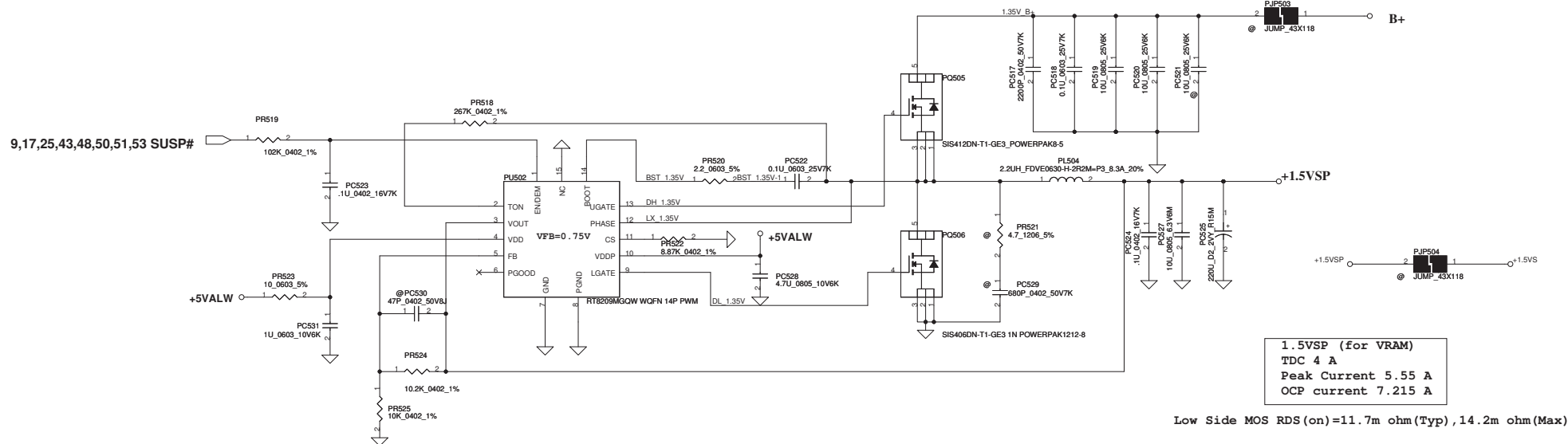
3.3VALWP  
TDC 6.5 A  
Peak Current 10.874 A  
OCP current 14.1A

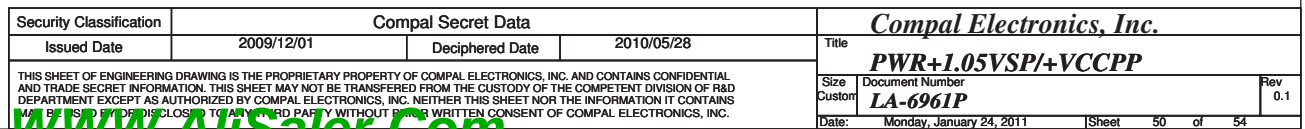
5VALWP  
TDC 5.7 A  
Peak Current 9.636 A  
OCP current 12.5A low side mos  
RDS 14.5m ohm 11.5m ohm

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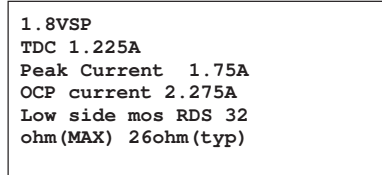


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Date:		Monday, January 24, 2011		Sheet 48 of 54

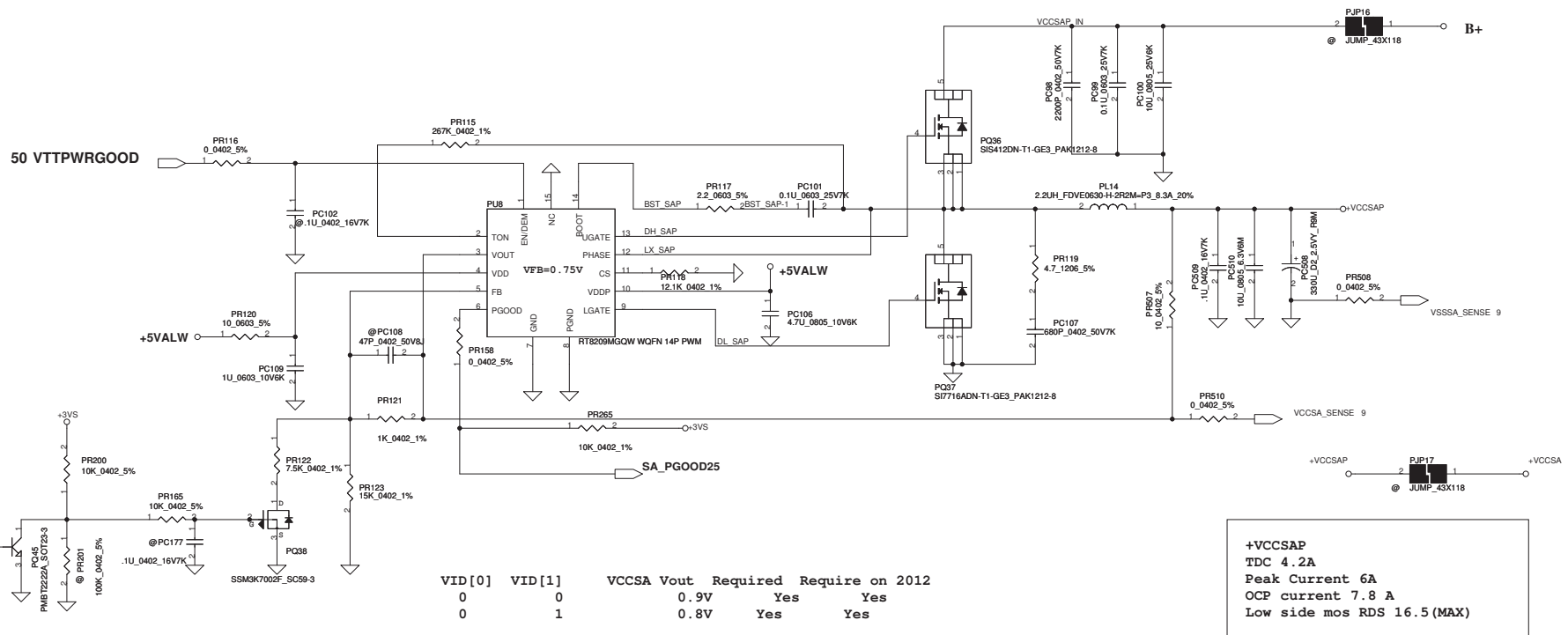




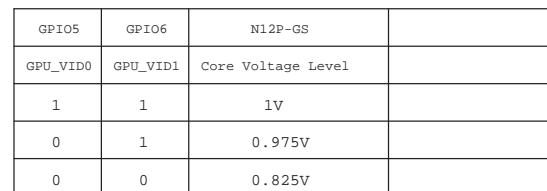




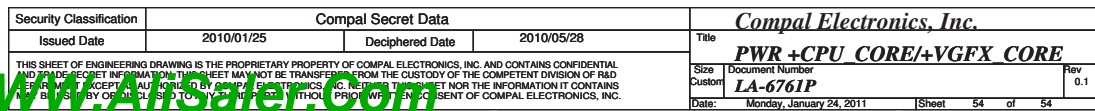
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				Date: Tuesday, January 25, 2011	Sheet 53 of 54	



Item	Reason for change	PG#	Modify List	Date	Phase
1	SYSON signal Pull low	43	Add R300	2010/10/15	PT
2	Q21 Reverse	25	Change Q21 DS pin	2010/10/15	PT
3	Fan voltage need to stable	26	Add C1923	2010/10/15	PT
4	Timing change	5	Add RC127,RC128,and Change BOM RC6 resrve	2010/10/15	PT
5	Leakge +3vs	13	Change BOM RH95 to resrve	2010/10/15	PT
6	EA crystal fail	25	Change BOM of C287,C288	2010/10/15	PT
7	EA crystal fail	13	Change BOM of CH23,CH24	2010/10/15	PT
8	EA crystal fail	21	Change BOM of CL18,CL19	2010/10/15	PT
9	High pot	21	Change CL39 to SB120102KIL	2010/10/15	PT
10	DPX request	42	Change JKB1 symbol	2010/10/15	PT
11	ME request	23	Change JBT1 symbol	2010/10/15	PT
12	PCB change version	12	Change BOM UHI SA00004IV0L	2010/10/15	PT
13	Control LAN LED limiting light	21	Add series connection RL26,RL25,Change BOM RL20 to 0ohm	2010/10/17	PT
14	HuronRiver DG updated for HAD_SYNC pull-down 1M ohm	12	Add RH275 resistor connect to HDA_SYNC_R & GND	2010/10/17	PT
15	Control the LCD sequence for AUO requirement	20	Add R2005,R2006 to reserve EN_INVFWR & +LCDVDD solution	2010/10/17	PT
16	Control the LCD sequence for AUO requirement	20	Add R2013,R2014,Q305 to reserve INVFWR_B+ Discharg Circuit	2010/10/20	PT
17	USB3.0 controller change to UPD720200AFIDAPA	24	Add R1962,R1963 to UPD720200AFIDAPA solution	2010/10/20	PT
18	NV request	28	Change R463,R465 pin2 net to +3VS_BOPU	2010/10/22	PT
19	NV request	33	Change BOM of RV109,RV116 to 1Kohm	2010/10/22	PT
20	The double pull low	29	Change BOM R937 to resrve	2010/10/22	PT
21	Modify screw H18 for ME request	39	Change H18 symbol	2010/10/22	PT
22	The EC request	25	Change RI095 to EC_CRY2 net,	2010/10/22	PT
23	The EC request	25	Change BOM R253 to 0ohm,RI095 to 100Kohm,C287,C288, XI resrve	2010/10/24	PT
24	The EC request	25	Change BOM R225 to 8.2kohm	2010/10/24	PT
25	The EC request	25	Change R222 to D7I	2010/10/26	PT
26	Intel request	12-19	Change BOM UHI SA00004IVIL	2010/12/1	ST
27	Changed from +3vs to +valw to fix issue can't wake from S3 by port of USB3.0	24	Change BOM Del R1963 ,Add R1962	2010/12/1	ST
28	NV request	41	Change BOM RV88 to 4.99K ohm	2010/12/1	ST
29	Maximum derateing changed from 12V to 20V	9	Change BOM QC4 to SB00000HK0L	2010/12/1	ST
30	Maximum derateing changed from 2V to 2.5V	9	Change BOM CC176 to SGA00005H0L	2010/12/1	ST
31	EMI request	20	Add L5 to SM01000DH0L	2010/12/6	ST
32	EMI request	20	Change BOM CU63 to 100PF	2010/12/6	ST
33	EMI request	20	Change BOM C1167 to 22PF	2010/12/6	ST
34	GLAN orange LED too dark	21	Change BOM RL26 to 200ohm	2010/12/6	ST
35	The EC request	25	Add C1947 to SB07I200J6L	2010/12/8	ST
36	The safety request	12	Change DH4 pin1,2,3	2010/12/8	ST
37	The USB3_SMI# signal change to GPIO14	15	Change UH1 pin C23 and H15	2010/12/8	ST
38	The DP Power Dongle	29	Add C110	2010/12/8	ST
39	The ME request	8	Change BOM C110 to C112	2010/12/9	ST
40	For ENE EC protect	20	17I2 add D13, R395		
41					
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2009/07/25		2010/07/25		HW Changed-List History-1		
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					LA-6961P	0.3
				Date:	Monday, January 24, 2011	Sheet 55 of 55